

# KR CS MLK 13" Schematics Whiskey Lake-U

**2018-07-19**  
**REV : A00**

***DY : None Installed***  
***UMA: UMA only installed***

<Core Design>



**Wistron Corporation**  
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Title

***Cover Page***

Size  
A4

Document Number

**KR CS MLK 13"**

Rev

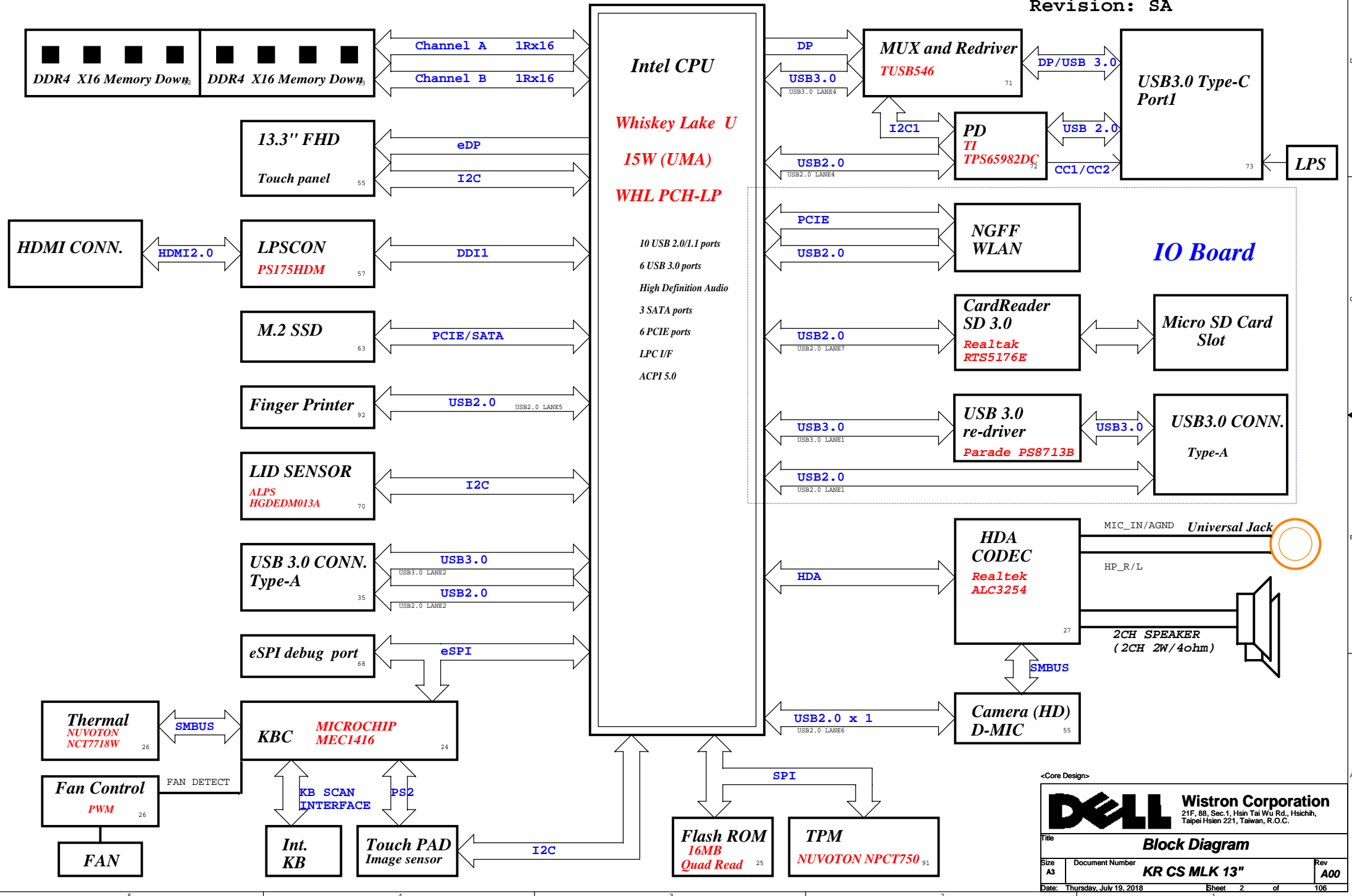
**A00**

Date: Thursday, July 19, 2018

Sheet 1 of 106

# WHL-U 13" CPU 15W Block Diagram

Project code: 4PD0EZ010001???  
PCB P/N: 17945  
Revision: SA





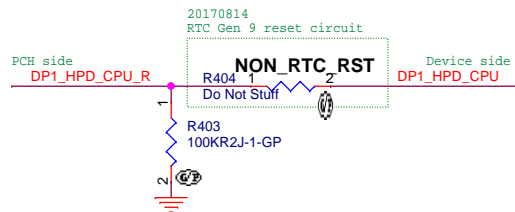
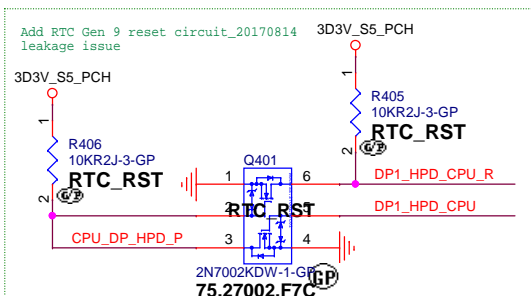
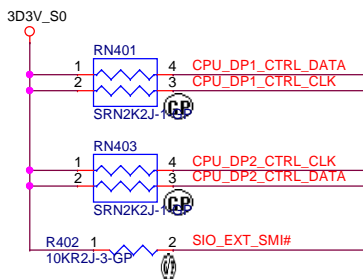
# SSID = CPU

## DP to HDMI2.0

[57] HDMI\_DDI\_TX\_N0 <<<  
[57] HDMI\_DDI\_TX\_P0 <<<  
[57] HDMI\_DDI\_TX\_N1 <<<  
[57] HDMI\_DDI\_TX\_P1 <<<  
[57] HDMI\_DDI\_TX\_N2 <<<  
[57] HDMI\_DDI\_TX\_P2 <<<  
[57] HDMI\_DDI\_TX\_N3 <<<  
[57] HDMI\_DDI\_TX\_P3 <<<  
[57] DP1\_AUX\_CPU\_N <<<  
[57] DP1\_AUX\_CPU\_P <<<  
[57] HDMI\_HPD\_CPU >>>

## DP for Type-C Mux

[71] DP2\_DDI\_TX\_N0 <<<  
[71] DP2\_DDI\_TX\_P0 <<<  
[71] DP2\_DDI\_TX\_N1 <<<  
[71] DP2\_DDI\_TX\_P1 <<<  
[71] DP2\_DDI\_TX\_N2 <<<  
[71] DP2\_DDI\_TX\_P2 <<<  
[71] DP2\_DDI\_TX\_N3 <<<  
[71] DP2\_DDI\_TX\_P3 <<<  
[71] DP2\_AUX\_CPU\_N <<<  
[71] DP2\_AUX\_CPU\_P <<<  
[55] eDP\_TX\_CPU\_N0 <<<  
[55] eDP\_TX\_CPU\_P0 <<<  
[55] eDP\_TX\_CPU\_N1 <<<  
[55] eDP\_TX\_CPU\_P1 <<<  
[55] eDP\_TX\_CPU\_N2 <<<  
[55] eDP\_TX\_CPU\_P2 <<<  
[55] eDP\_TX\_CPU\_N3 <<<  
[55] eDP\_TX\_CPU\_P3 <<<  
[55] eDP\_AUX\_CPU\_N <<<  
[55] eDP\_AUX\_CPU\_P <<<  
[55] eDP\_HPD\_CPU <<<  
[71,72] DP1\_HPD\_CPU <<<  
[24] L\_BKLT\_EN <<<  
[55] L\_BKLT\_CTRL <<<  
[55] EDP\_VDD\_EN <<<  
[15] GPP\_H17\_STRAP >>>



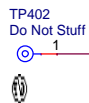
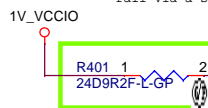
### (#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC

## DP to HDMI2.0

## DP for Type-C Mux

CHECK WHL design guide: DISP\_RCOMP  
Design Guideline:  
Skylake processor signal eDP\_RCOMP  
should be connected to the VCCIO  
rail via a single 24.9 ±1% Q resistor.



### (#543016) eDP\_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ±1%	Max = 100 mils

HDMI\_DDI\_TX\_N0 AL5  
HDMI\_DDI\_TX\_P0 AL6  
HDMI\_DDI\_TX\_N1 AJ5  
HDMI\_DDI\_TX\_P1 AJ6  
HDMI\_DDI\_TX\_N2 AF6  
HDMI\_DDI\_TX\_P2 AF5  
HDMI\_DDI\_TX\_N3 AE5  
HDMI\_DDI\_TX\_P3 AE6  
DP2\_DDI\_TX\_N0 AC4  
DP2\_DDI\_TX\_P0 AC3  
DP2\_DDI\_TX\_N1 AC1  
DP2\_DDI\_TX\_P1 AC2  
DP2\_DDI\_TX\_N2 AE4  
DP2\_DDI\_TX\_P2 AE3  
DP2\_DDI\_TX\_N3 AE1  
DP2\_DDI\_TX\_P3 AE2

CPU1A  
DDI1\_TXN0  
DDI1\_TXP0  
DDI1\_TXN1  
DDI1\_TXP1  
DDI1\_TXN2  
DDI1\_TXP2  
DDI1\_TXN3  
DDI1\_TXP3  
DDI2\_TXN0  
DDI2\_TXP0  
DDI2\_TXN1  
DDI2\_TXP1  
DDI2\_TXN2  
DDI2\_TXP2  
DDI2\_TXN3  
DDI2\_TXP3

1 OF 20  
EDP\_TXN0 AG4  
EDP\_TXP0 AG3  
EDP\_TXN1 AG2  
EDP\_TXP1 AG1  
EDP\_TXN2 AJ4  
EDP\_TXP2 AJ3  
EDP\_TXN3 AJ2  
EDP\_TXP3 AJ1

EDP\_AUX\_N AH4  
EDP\_AUX\_P AH3

DISP\_UTILS AM7  
DDI1\_AUX\_N AC7  
DDI1\_AUX\_P AC6  
DDI2\_AUX\_N AD4  
DDI2\_AUX\_P AD3  
DDI3\_AUX\_N AG7  
DDI3\_AUX\_P AG6

GPP\_E13/DDPB\_HPD0/DISP\_MISC0  
GPP\_E14/DDPC\_HPD1/DISP\_MISC1  
GPP\_E15/DPPD\_HPD2/DISP\_MISC2  
GPP\_E16/DPPD\_HPD3/DISP\_MISC3  
GPP\_E17/EDP\_HPD/DISP\_MISC4

EDP\_BKLTEN  
EDP\_VDDEN  
EDP\_BKLTCTL

DISP\_RCOMP

GPP\_E18/DPPB\_CTRLCLK/CNV\_BT\_HOST\_WAKE#  
GPP\_E19/DPPB\_CTRLDATA

GPP\_E20/DPPC\_CTRLCLK  
GPP\_E21/DPPC\_CTRLDATA

GPP\_E22/DPPD\_CTRLCLK  
GPP\_E23/DPPD\_CTRLDATA

GPP\_H16/DDPF\_CTRLCLK  
GPP\_H17/DDPF\_CTRLDATA

WHISKEY-LAKE-GP

CN6 HDMI\_HPD\_CPU  
CM6 DP1\_HPD\_CPU\_R  
CP7 SIO\_EXT\_SMI#  
CP6 eDP\_HPD\_CPU  
CM7  
CK11 L\_BKLT\_EN  
CG11 EDP\_VDD\_EN  
CH11 L\_BKLT\_CTRL

20180208  
Follow RO NC  
for HDMI2.0  
for Type-C Mux

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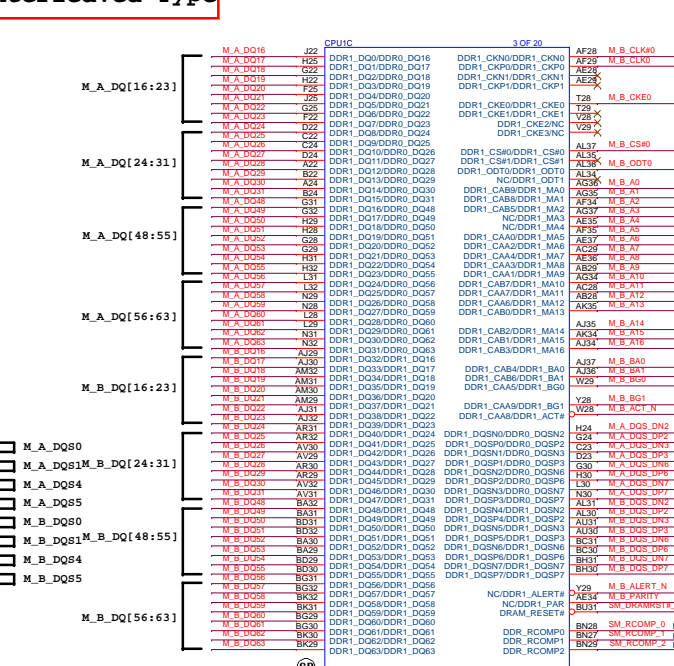
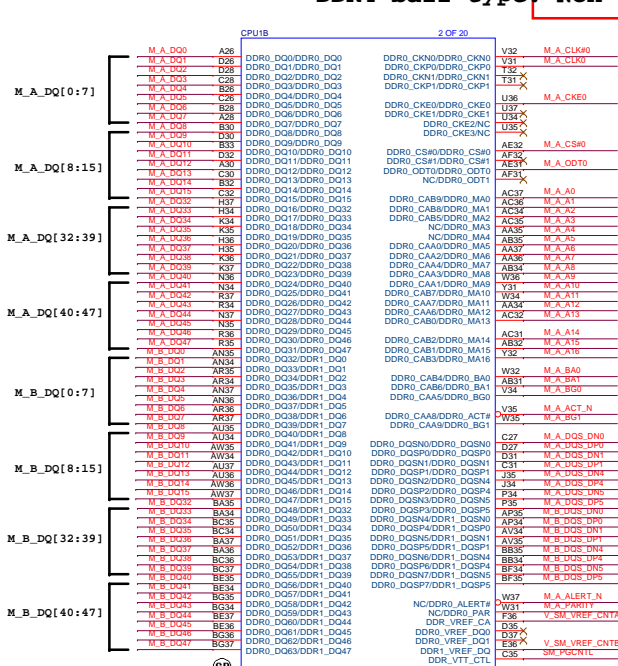
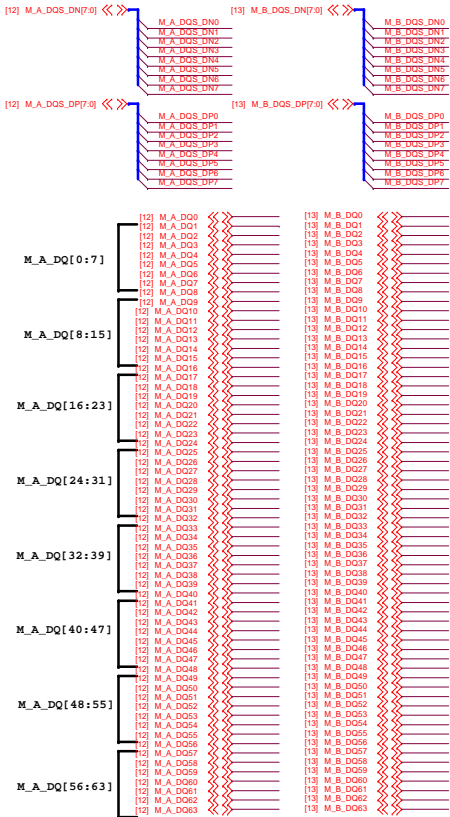
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Title CPU\_(JTAG/CPU SIDE BAND)

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SSID = CPU

## DDR4 ball type: Non-Interleaved Type



WHISKEY-LAKE-GP

DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel.  
Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.

### 6.3.8 Coffee Lake U PDG x8 and x16 memory Down Routing Guidelines is Updated

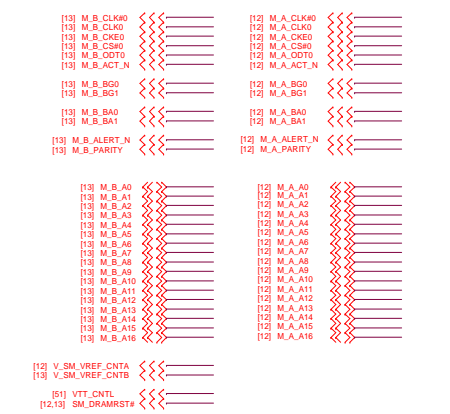
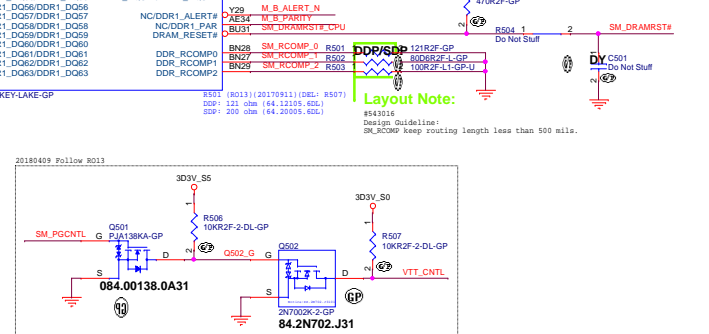
Coffee Lake U PDG (IBP #571021) x8 and x16 memory down routing guidelines has been updated.

Chapter 4.3.2 Table 4-12 CFL U DDR4 x16 Memory Down Routing Guidelines (mils):

- Rcomp [0] = 200/121
- Rcomp [1] = 80.6
- Rcomp [2] = 100

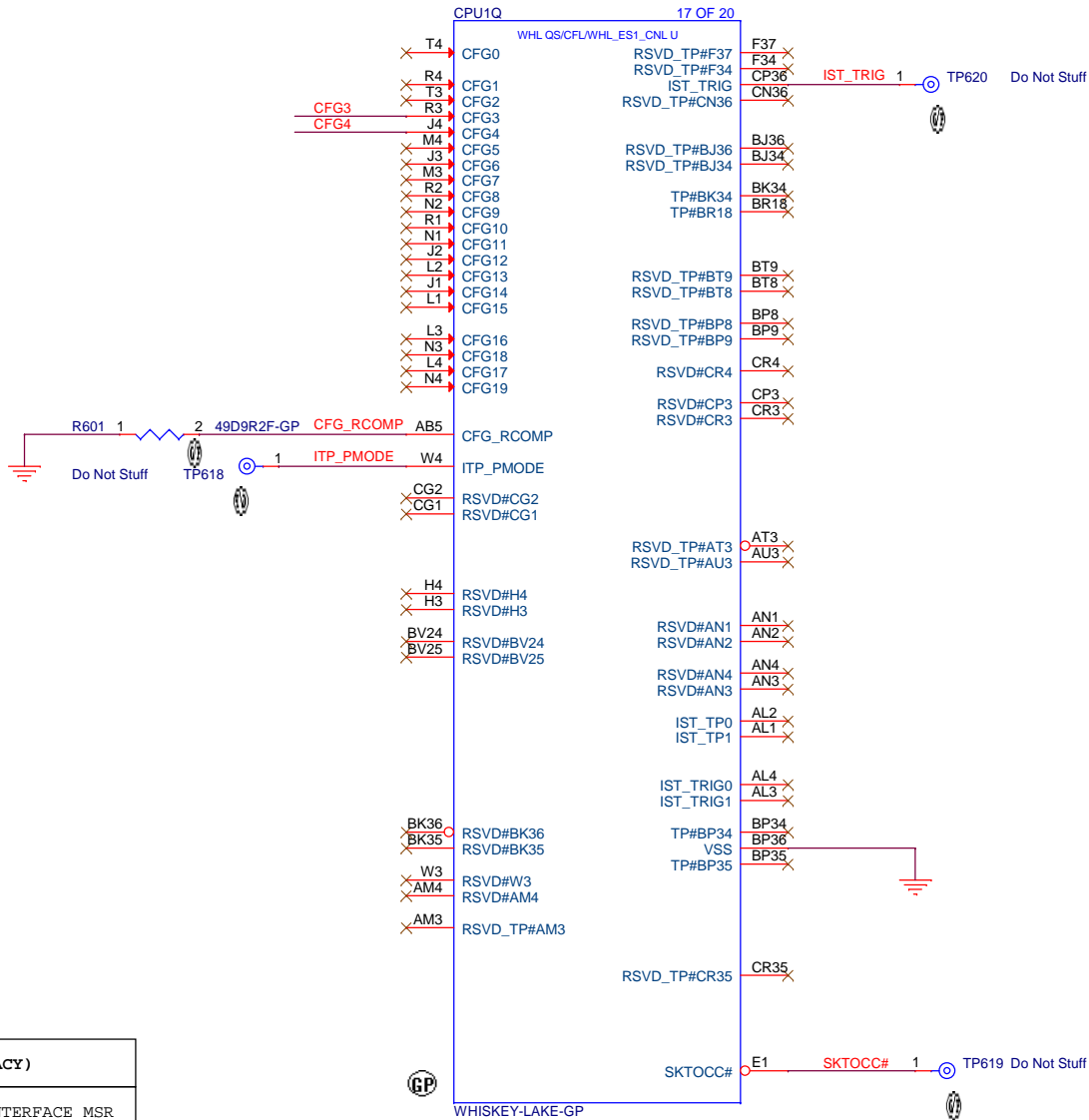
Chapter 4.3.3 Table 4-16 CFL U DDR4 x8 Memory Down Routing Guidelines (mils):

- Rcomp [0] = 121
- Rcomp [1] = 80.6
- Rcomp [2] = 100



SSID = CPU

[15] CFG3 <<>>  
[15] CFG4 <<>>



### PCH strap pin:

CFG3 CFG4

[BDW Only]PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR
	1 : DISABLED

(#543016)  
SKL(#543016):  
Processor strap CFG[4] should be pulled low to enable embedded DisplayPort\*

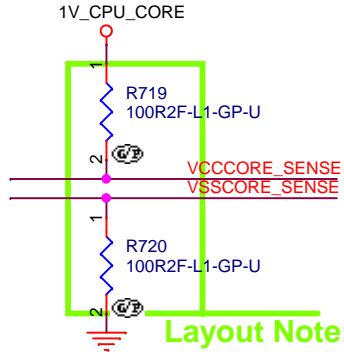
DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port.
	1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.

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<b>CPU (RESERVED)</b>			
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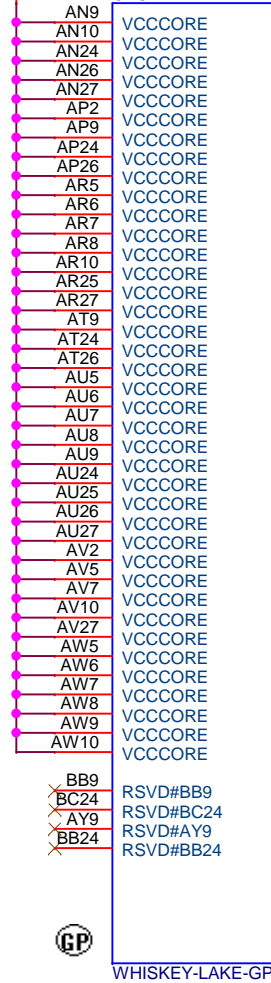
# SSID = CPU

[46] VCCCORE\_SENSE <<< <<<  
[46] VSSCORE\_SENSE <<< <<<  
[46] SVID\_CLK\_CPU <<< <<<  
[46] SVID\_ALERT#\_CPU <<< <<<  
[46] SVID\_DATA\_CPU <<< <<<



1. Place close to CPU
2. VCC\_SENSE/ VSS\_SENSE impedance=50 ohm
3. Length match<25mil

1V\_CPU\_CORE



VCC\_SENSE  
VSS\_SENSE  
VIDALERT#  
VIDSK  
VIDSOUT  
RSVD#Y3  
VCCSTG

## SVID\_543016:

Layout Note:  
The total Length of Data and Clock (from CPU to each VR) must be equal ( $\pm 0.1$  inch).  
Route the Alert signal between the Clock and the Data signals.

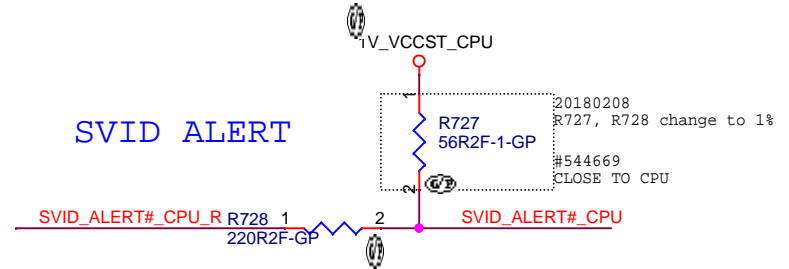
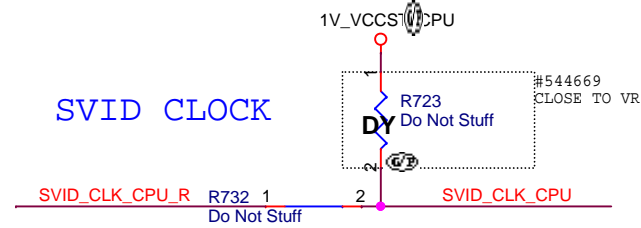
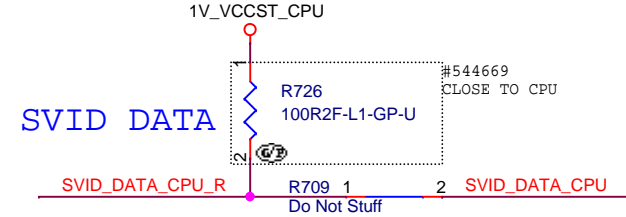


Figure 10-7. Routing Illustration for SVID Topology

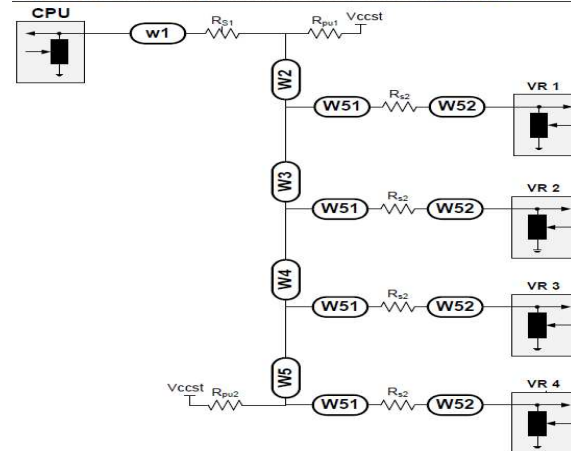


Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R001 [Ω]	R002 [Ω]	R01 [Ω]	R02 [Ω]	VCCST [v]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSK							Empty	45	0	50	
VIDALERT #							56	Empty	220	0	

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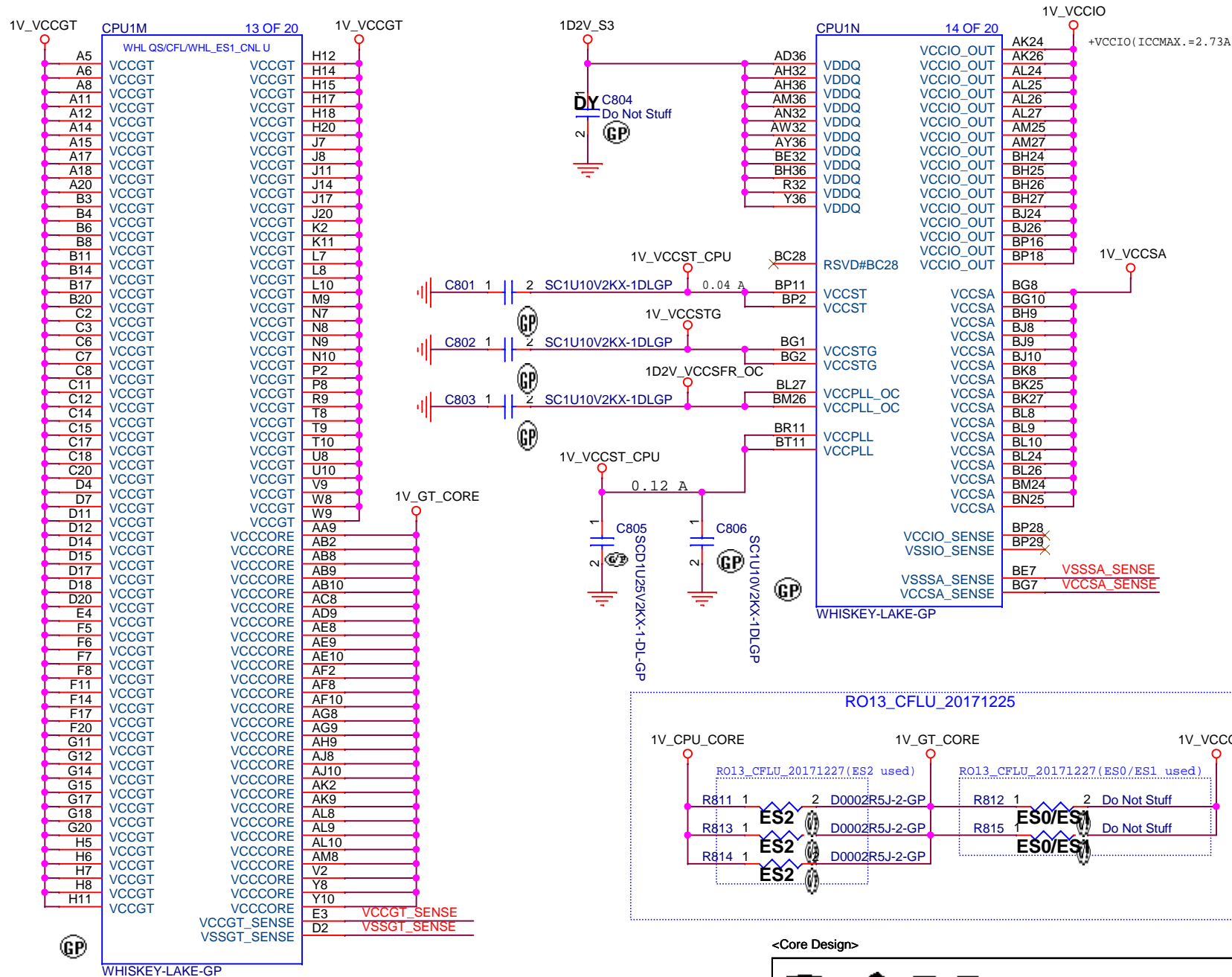
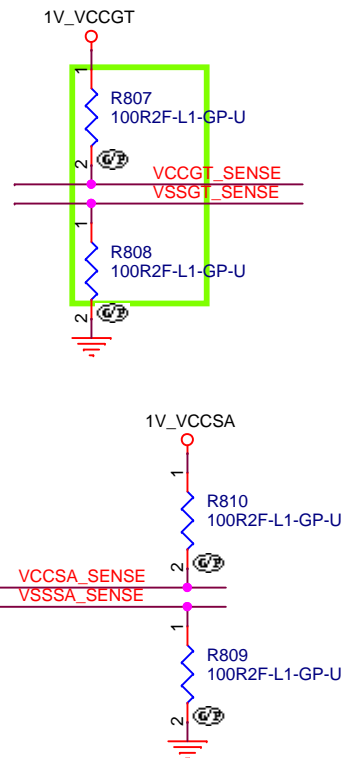


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[46] VCCGT\_SENSE <<< \_\_\_\_\_  
[46] VSSGT\_SENSE <<< \_\_\_\_\_  
[46] VSSSA\_SENSE <<< \_\_\_\_\_  
[46] VCCSA\_SENSE <<< \_\_\_\_\_



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**CPU (DISPLAY)**

Size  
A4

Document Number

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# SSID = CPU

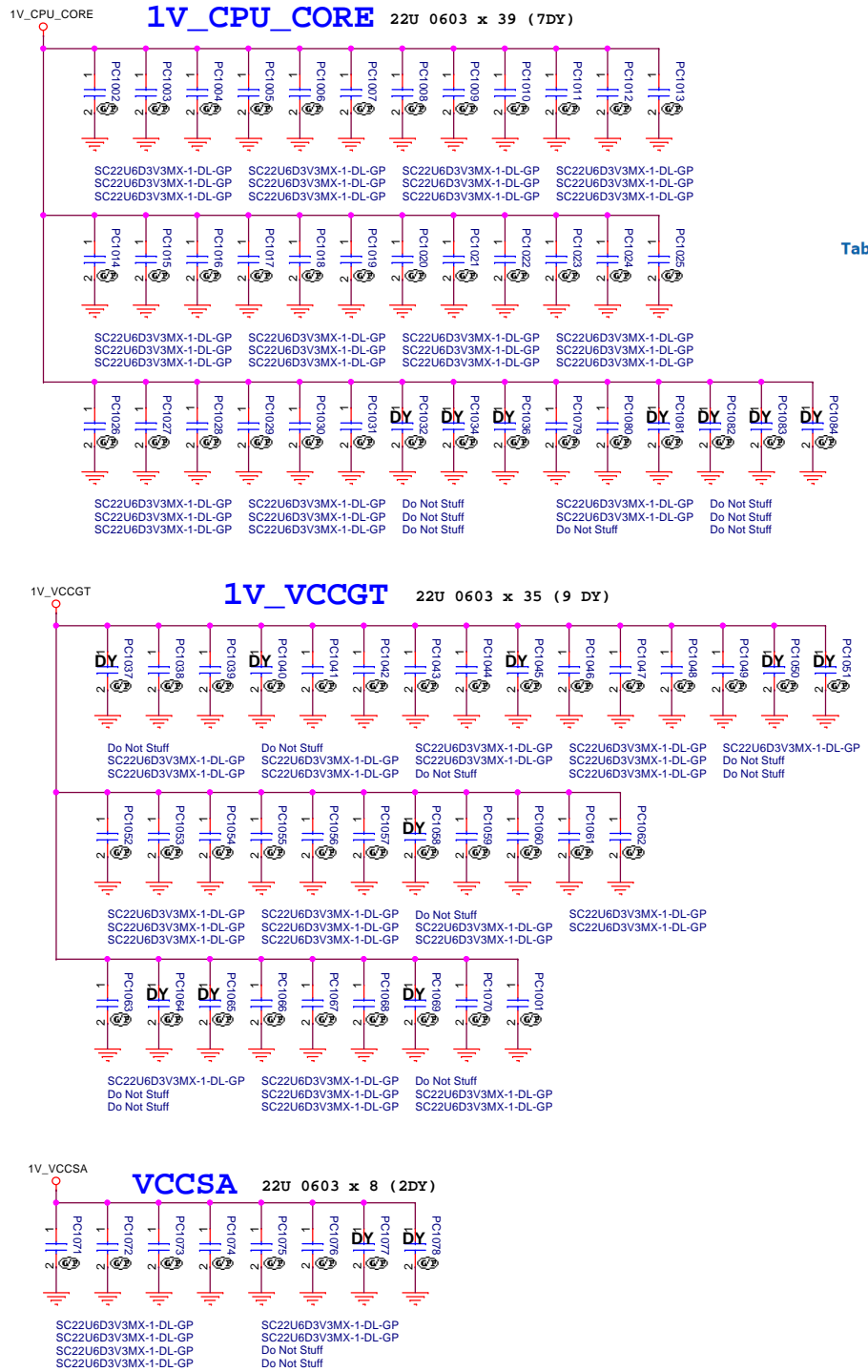


Table 11-5. Whiskey Lake U 4+2/Whiskey Lake U 4+2f/Cannon Lake U 2+2/ Coffee Lake U 4+3e Bulk Decoupling Example

Bulk Decoupling Locations	Example WHL U42	Example WHL U42f	Example CNL U22	Example CFL U43e	Notes
VCC <sub>core</sub> Power Plane at VR output	4x 220uF (@4.5mO ESR)	3x 220uF (@4.5mO ESR)	TBD	3x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
VCC <sub>GT</sub> Power Plane at VR output	4x 220uF (@4.5mO ESR)	2x 220uF (@4.5mO ESR)	TBD	4x 220uF (@4.5mO ESR)	Placed at primary side near to VR output

**Notes:**

- These examples are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.
- Bulk decoupling is not a "requirement" but recommendation only. It is an example of VR design/VR bandwidth. Customer should work with respective vendor to validate their VR & bulk decoupling designs to ensure the electrical requirements are met.

Table 11-6. Decoupling Requirements for Whiskey Lake U 4+2/Coffee Lake U 4+2f/ Cannon Lake U 2+2/ Coffee Lake U 4+3e Processor (Sheet 1 of 2)

Domain	Primary Side cap	Secondary Side cap	Placement guideline
VCC <sub>core</sub>		35x 1uF 0402/0201	To be placed as close as possible to the vias that connect to the BGA pins.
		14x 10uF 0402	
		9x 22uF 0603	
	8x 10uF 0402		Place as close to the package as possible
VCC <sub>core</sub> -VCC <sub>GT</sub> ISLAND		18x 47uF 0805 (6.3V)	Place as close to the package as possible. Can be placed on as either Primary or back side cap.
		7x 1uF 0402/0201	Place as close as possible to the package.
		7x 10uF 0402	

Table 11-6. Decoupling Requirements for Whiskey Lake U 4+2/Coffee Lake U 4+2f/ Cannon Lake U 2+2/ Coffee Lake U 4+3e Processor (Sheet 2 of 2)

Domain	Primary Side cap	Secondary Side cap	Placement guideline
VCC <sub>GT</sub>		11x 1uF 0402/0201	Place as close to the package as possible
		15x 10uF 0402	
	15x 22uF 0603		
	8x 47uF 0805 (6.3V)		
	7x 0603		Placeholder only
VCC <sub>SA</sub>	2x 0805		Placeholder only
		7x 1uF 0201	Place as close to the package as possible
		9x 10uF 0402	
	6x 10uF 0402		
	2x 47uF 0805 (6.3V)		
VDD <sub>Q</sub>	2x 0805		Placeholder Only
		4x 1uF 0402/0201	Place as close to the package as possible.
		3x 10uF 0402	
	1x 22uF 0603		
	6x 10uF 0402		
VCC <sub>IO</sub>	4x 1uF 0201		Place as close to the package as possible
		4x 1uF 0402/0201	Place as close to the package as possible
		6x 10uF 0402	
	4x 0402		Placeholder Only
	1x 1uF 0402		
VCC <sub>PULL</sub> OC	1x 1uF 0402		Do not merge VCC <sub>PULL</sub> , VCC <sub>PULL</sub> OC and VCC <sub>GT</sub> to any noisy and high current power rail and do not route them close/ adjacent to and reference to, any noisy and high current rail on top and bottom layers - as this may impact to PULL falling to phase lock.
	1x 0.1uF 0201		Place as close as possible to BGA.
	1x 1uF 0402		Place as close as possible to BGA and can be placed on as either Primary or backside cap.
		1x 0805	Placeholder Only. Can be placed on as either Primary or back side cap.
VCC <sub>GT</sub>	1x 1uF 0402		
VCC <sub>GTG</sub>	1x 1uF 0402		
VCC <sub>BIOSS</sub>		6x 1uF 0201	Place as close to the package as possible.
		2x 22uF 0603	VCC <sub>BIOSS</sub> and VCC <sub>OC</sub> rails are merged on board. VT to be placed as close as possible to BGA and a wide plane routing to meet DC_R <= 7mOhm.
		4x 10uF 0402	VCC <sub>BIOSS</sub> and VCC <sub>OC</sub> is required for CFL-U43e SKUs only.
VCC <sub>OC</sub>		2x 22uF 0603	

**Notes:**

- The 6.3V voltage is for the higher capacitance retention; more 0805 components will be required for a lower voltage capacitor rating. Assumption: VR loop bandwidth ~ 250kHz e.g., 1MHz switching VR
- Component placement order: Package edge > 0402 caps > 0603 caps > 0805 caps > Bulk caps > Power source.

Figure 11-10. Whiskey Lake U 4+2f/Cannon Lake U 2+2/ Coffee Lake U 4+3e Processor - Power/Ground pin PTH/via Pattern Guideline

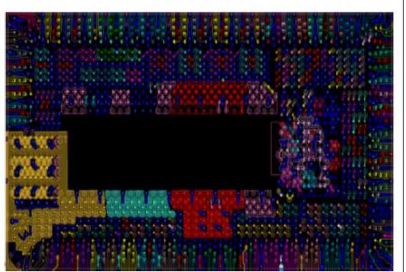
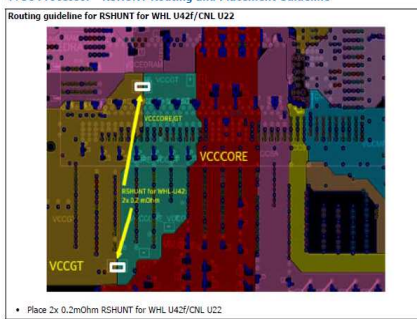



Figure 11-11. Whiskey Lake U 4+2/Coffee Lake U 4+2f/Cannon Lake U 2+2/ Coffee Lake U 4+3e Processor - RSHUNT Routing and Placement Guideline



Figure 11-11. Whiskey Lake U 4+2/Coffee Lake U 4+2f/Cannon Lake U 2+2/ Coffee Lake U 4+3e Processor - RSHUNT Routing and Placement Guideline



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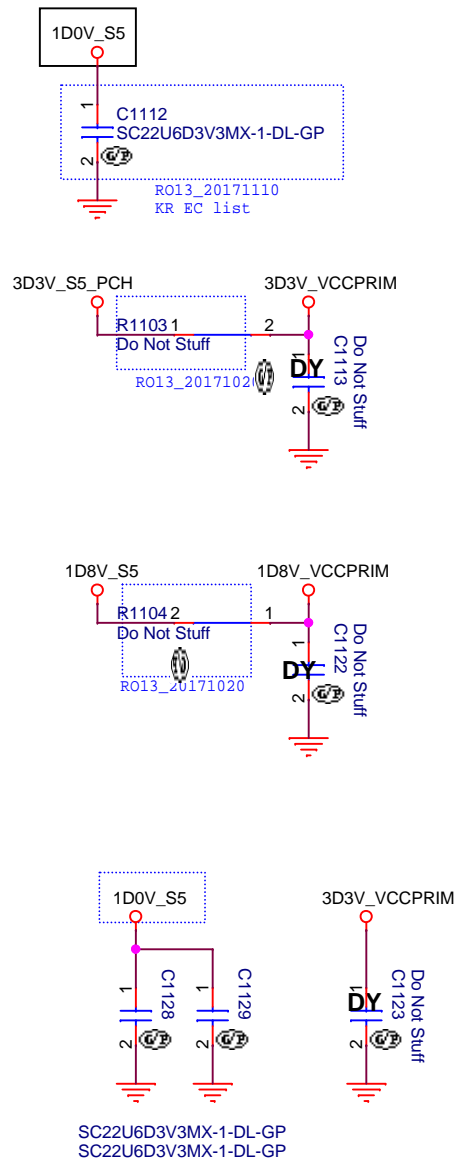
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Title: **CPU (Power CAP1)**

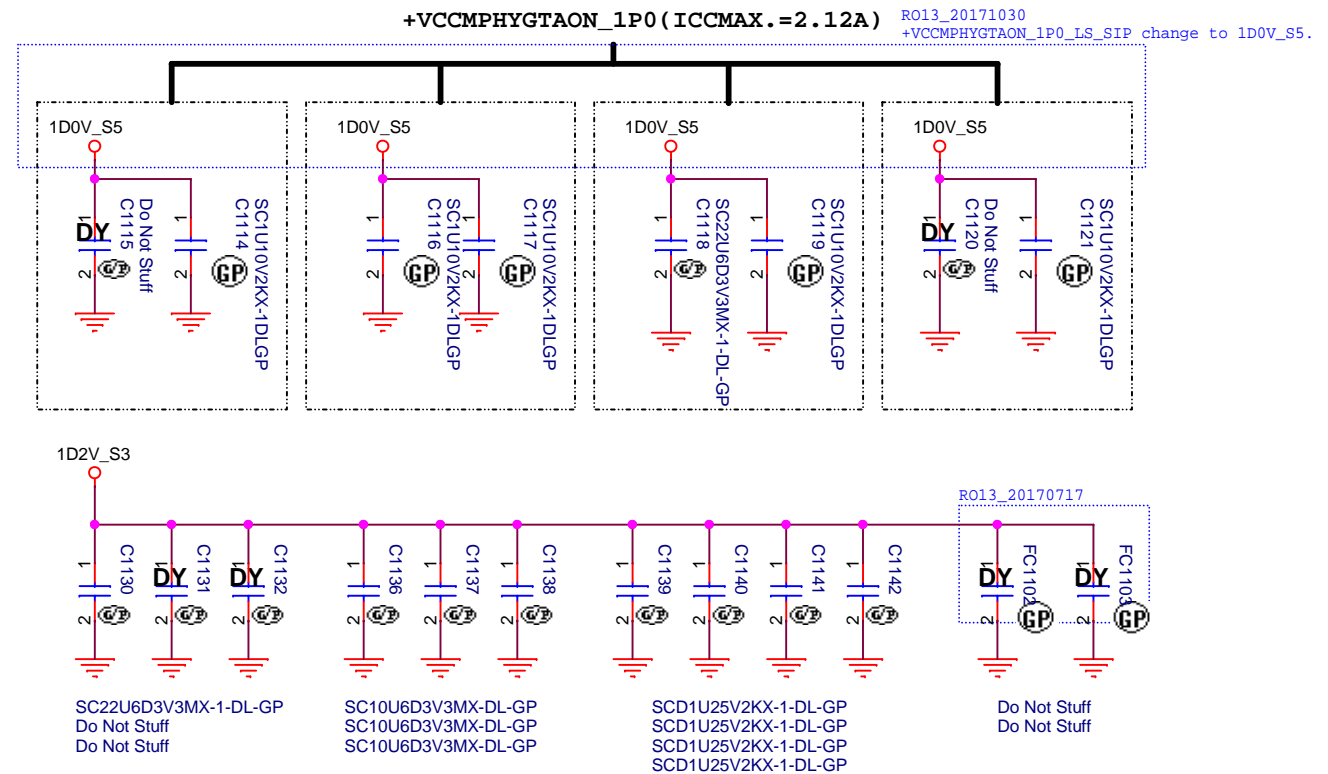
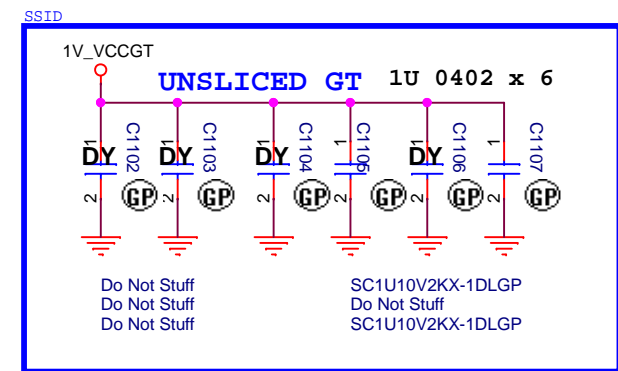
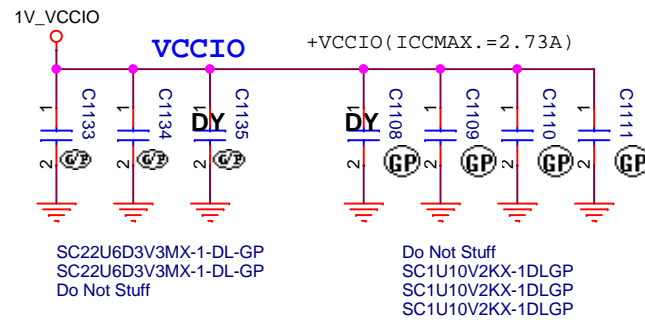
Size A3	Document Number: <b>KR CS MLK 13"</b>	Rev: <b>A00</b>
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# SSID = CPU

## PCH Power



## CPU Power

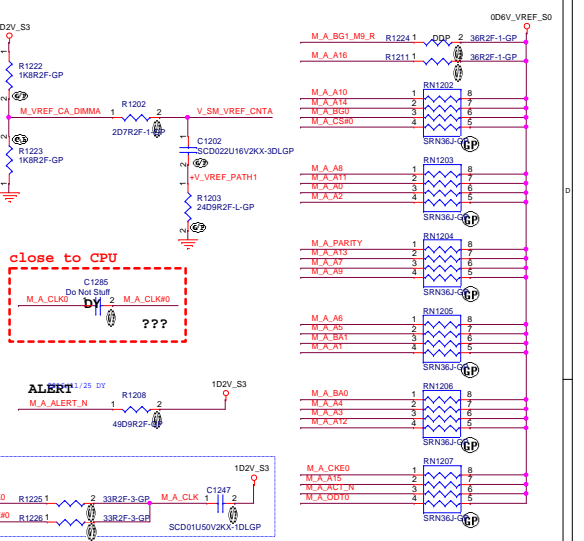
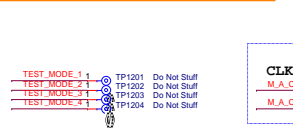
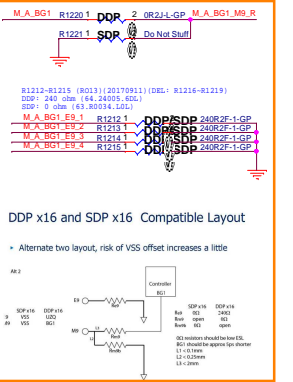
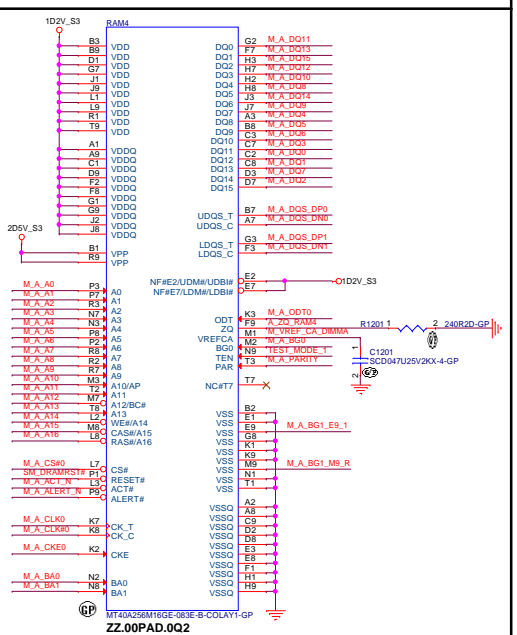
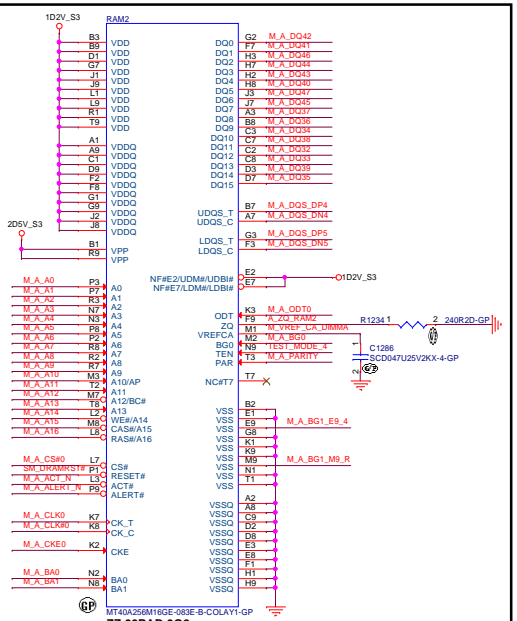
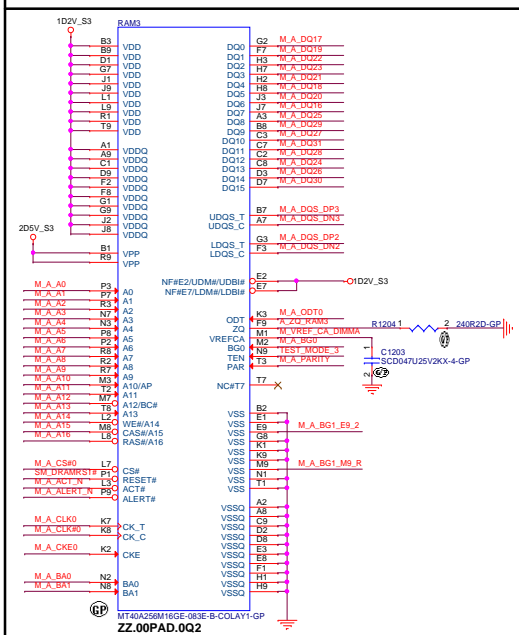
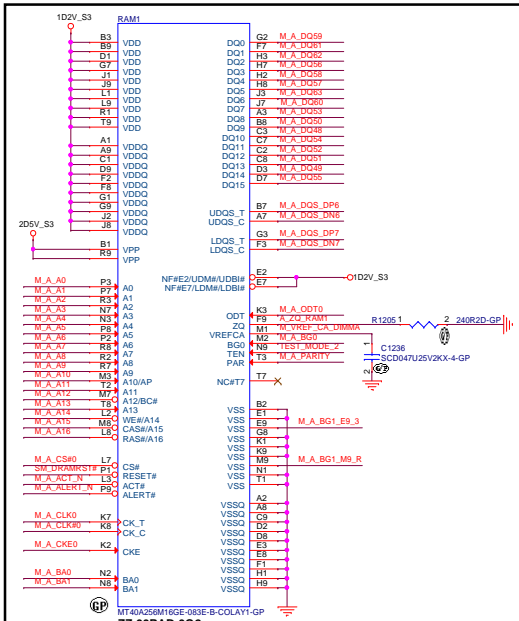
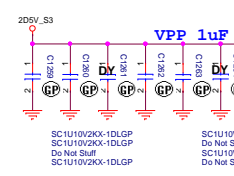
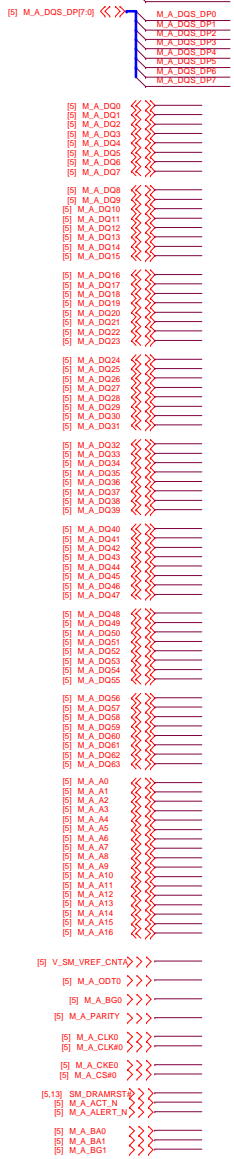


<Core Design>

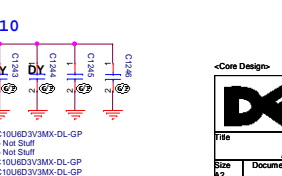
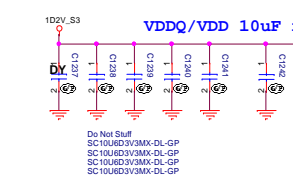
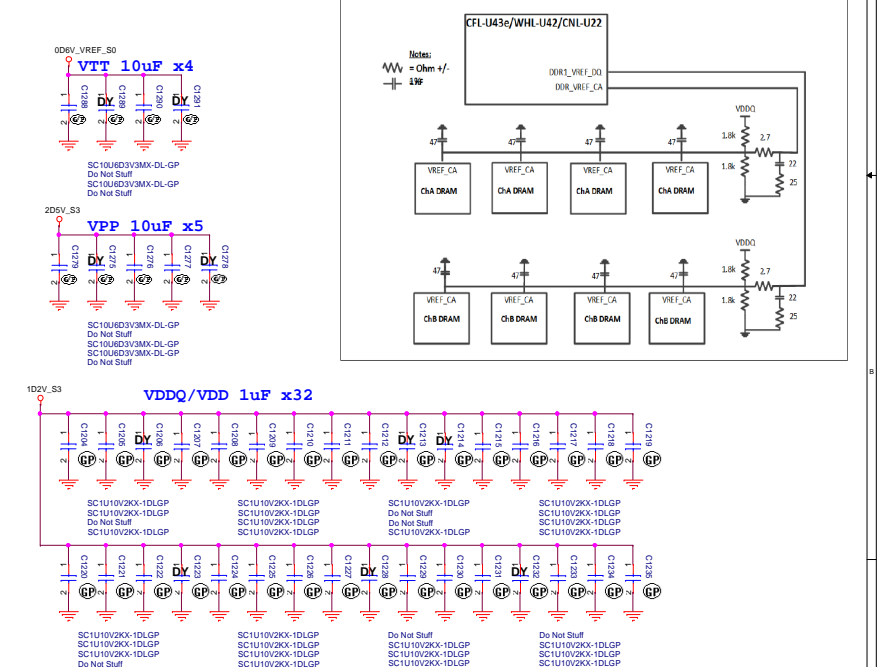
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>CPU (Power CAP2)</b>			
Size A4	Document Number <b>KR CS MLK 13"</b>		Rev <b>A00</b>
Date: Thursday, July 19, 2018		Sheet 11	of 106

[5] M\_A\_DQS\_DN[7:0] << >>

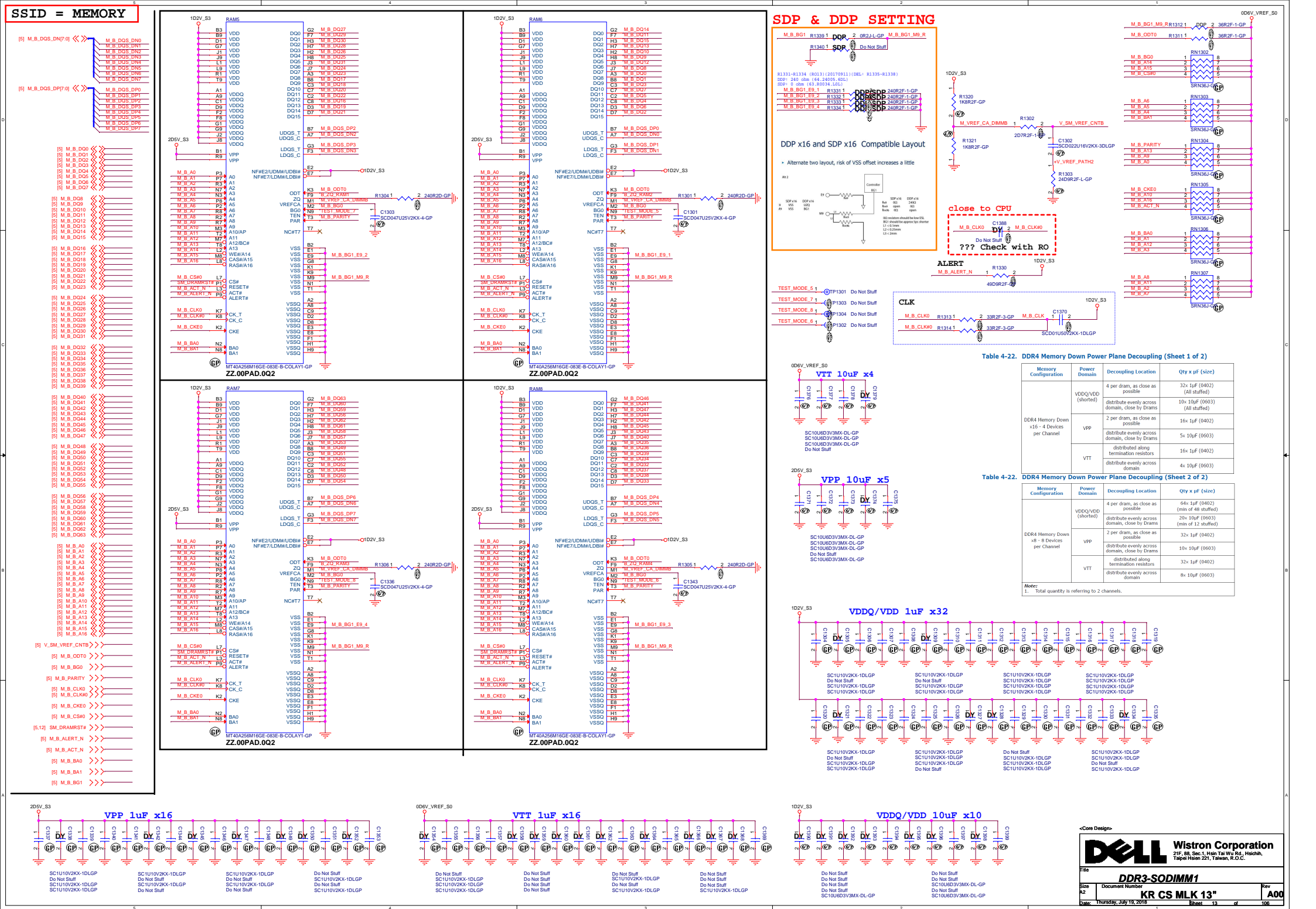
The diagram shows a blue bus line labeled [5] M\_A\_DQS\_DN[7:0] << >> on the left. This bus connects to a vertical stack of seven horizontal lines, each labeled with a DQS signal: M\_A\_DQS\_DN0, M\_A\_DQS\_DN1, M\_A\_DQS\_DN2, M\_A\_DQS\_DN3, M\_A\_DQS\_DN4, M\_A\_DQS\_DN5, and M\_A\_DQS\_DN6. The signal M\_A\_DQS\_DN7 is not shown in this diagram.



**Figure 4-8. WHL U DDR4 x16 Devices Memory Down V<sub>REF-CA</sub> Overview**







( Blanking )

<Core Design>

			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>(Reserved)_SODIMM _SODIMM4</b>					
Size A4		Document Number <b>KR CS MLK 13"</b>			Rev <b>A00</b>
Date: Thursday, July 19, 2018		Sheet 14		of 106	

15122	0x00	00000000
15123	0x00	00000000
15124	0x00	00000000
15125	0x00	00000000
15126	0x00	00000000
15127	0x00	00000000
15128	0x00	00000000
15129	0x00	00000000
15130	0x00	00000000
15131	0x00	00000000
15132	0x00	00000000
15133	0x00	00000000
15134	0x00	00000000
15135	0x00	00000000
15136	0x00	00000000
15137	0x00	00000000
15138	0x00	00000000
15139	0x00	00000000
15140	0x00	00000000
15141	0x00	00000000
15142	0x00	00000000
15143	0x00	00000000
15144	0x00	00000000
15145	0x00	00000000
15146	0x00	00000000
15147	0x00	00000000
15148	0x00	00000000
15149	0x00	00000000
15150	0x00	00000000
15151	0x00	00000000
15152	0x00	00000000
15153	0x00	00000000
15154	0x00	00000000
15155	0x00	00000000
15156	0x00	00000000
15157	0x00	00000000
15158	0x00	00000000
15159	0x00	00000000
15160	0x00	00000000
15161	0x00	00000000
15162	0x00	00000000
15163	0x00	00000000
15164	0x00	00000000
15165	0x00	00000000
15166	0x00	00000000
15167	0x00	00000000
15168	0x00	00000000
15169	0x00	00000000
15170	0x00	00000000
15171	0x00	00000000
15172	0x00	00000000
15173	0x00	00000000
15174	0x00	00000000
15175	0x00	00000000
15176	0x00	00000000
15177	0x00	00000000
15178	0x00	00000000
15179	0x00	00000000
15180	0x00	00000000
15181	0x00	00000000
15182	0x00	00000000
15183	0x00	00000000
15184	0x00	00000000
15185	0x00	00000000
15186	0x00	00000000
15187	0x00	00000000
15188	0x00	00000000
15189	0x00	00000000
15190	0x00	00000000
15191	0x00	00000000
15192	0x00	00000000
15193	0x00	00000000
15194	0x00	00000000
15195	0x00	00000000
15196	0x00	00000000
15197	0x00	00000000
15198	0x00	00000000
15199	0x00	00000000

GPP_B14 / SPMR	The Shared Channel	Rising edge of PCH_PWROK
----------------	--------------------	--------------------------



GPP_B18 / GSPID_MOSI	No Reboot	Rising edge of PCH_PWROK
----------------------	-----------	--------------------------



GPP_C2 / SMBALERT#	TLS Confidentiality	Rising edge of RSMRST#
--------------------	---------------------	------------------------



GPP_C12 / SMIALERT# / PCHHOT#	Flash BIOS/BIOS	Rising edge of PCH_PWROK
-------------------------------	-----------------	--------------------------



GPP_C5 / SMIALERT#	eSPI or LPC	Rising edge of RSMRST#
--------------------	-------------	------------------------



SPID_MOSI	Reserved	Rising edge of RSMRST#
-----------	----------	------------------------



GPP_D12 / ISH_SPI_MOSI / GSPID_MOSI	Reserved	Rising edge of RSMRST#
-------------------------------------	----------	------------------------



GPP_B23 / SMIALERT# / PCHHOT#	Intel® DCI+O0B	Rising edge of RSMRST#
-------------------------------	----------------	------------------------



SPID_I02	Reserved	Rising edge of RSMRST#
----------	----------	------------------------



SPID_I03	Reserved	Rising edge of RSMRST#
----------	----------	------------------------



HDA_SDO / I2SD_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK
--------------------	------------------------------------	--------------------------



GPP_E19 / DDPB_CTRLDATA / CNV_BT_IF_SELECT	Display Port B Detected	Rising edge of PCH_PWROK
--	-------------------------	--------------------------



GPP_E21 / DDPB_CTRLDATA	Display Port C Detected	Rising edge of PCH_PWROK
-------------------------	-------------------------	--------------------------



GPP_E23 / DDPB_CTRLDATA	Display Port D Detected	Rising edge of PCH_PWROK
-------------------------	-------------------------	--------------------------



GPP_H17	Reserved	Rising edge of PCH_PWROK
---------	----------	--------------------------



GPP_H21	XTAL Frequency Select	Rising edge of RSMRST#
---------	-----------------------	------------------------



GPP_F6 / CNV_RGL_DT	M/L2 CNV Mode Select	Rising edge of RSMRST#
---------------------	----------------------	------------------------



INPUT3VSEL	3.0V Select	Input pin must always be driven to a valid logic level
------------	-------------	--



GPD7	Reserved	Rising edge of DSN_PWROK
------	----------	--------------------------



GPP_H23	eSPI Flash Sharing Mode	Rising edge of RSMRST#
---------	-------------------------	------------------------



[New Only] PHYSICAL_DISK_ENABLED (Disk Privacy)	
DISK[0]	0 - Disabled Set disk enabled bit in disk interface MIB
	1 - Disabled



(004010)	
DISPLAY PORT PRESENCE STRAP	
CP0[4]	0 = Disabled An external Display Port device is connected to the Embedded Display Port. 1 = Enabled No external Display Port device is connected.



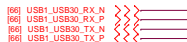


## SSID= PCH

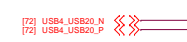
```
#543016:
220 nF nominal capacitors are recommended for Gen 3.
100 nF nominal capacitors are recommended for Gen 2.
```

```
(#545659) The xHCI controller supports USB Debug port on all USB3.0 capable ports.
```

### USB3.0



## USB2.0



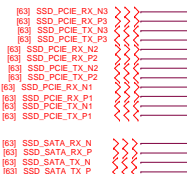
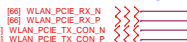
## OPTANE MEMORY



## SSD

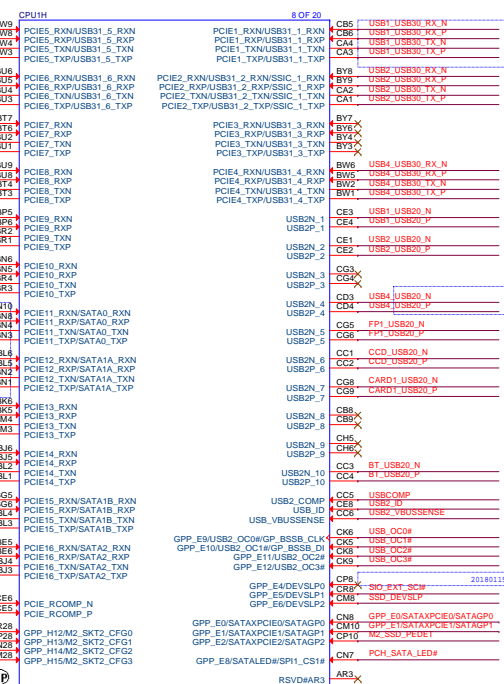


**PCIE**



**Figure 6-1. High Speed I/O (HSIO) Lane Multiplexing in CNL U PCH-LP**

Flex/I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	PCIe #7	PCIe #8	PCIe #9	PCIe #10	PCIe #11	PCIe #12	PCIe #13	PCIe #14	PCIe #15	PCIe #16
	PCIe #1	PCIe #2	PCIe #3	PCIe #4	PCIe #5	PCIe #6	QbE	QbE	QbE	SATA 0	SATA 1a	QbE	QbE	SATA 1b	SATA 2	SATA 3
Intel® RST Support	No Support			No Support			Yes			Yes						



- IO board USB3.0

MB USB3.0

## USB3.0 Type C

## IO board USB3.0

## MB USB3.0

USB3.0 Type C

Fingerprint Reader

## CAMERA

Card Reader

## WLAN (BT)

## IO USB3

### 5 Remove by



WHISKEY-LAKE-GP  
Layout Note:

1. Trace Width: 4 mils min (breakout) 12-15 mils (trace)  
Note: Must maintain low DC resistance routing (<0.1 ohm)
2. Isolation Spacing: At least 12 mils to any adjacent high speed I/O.

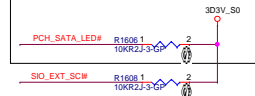
(#543016) Unused SATAGP[2:0]/GPP\_E[2:0] pins must be terminated to either 3.3 V rail or GND using 8.2 K $\Omega$  to 10 K $\Omega$  on the motherboard.  
Do not use both pull-up and pull-down. Either pull-up or pull-down is acceptable.

## USB 2.0 Table

Pair	Device
1	USB3.0 port1
2	N/A
3	USB3.0 Port2 (IOBD)
4	Type-c
5	CAMERA
6	WLAN
7	Touch Panel
8	Card Reader

#545659 (SKL\_PCH\_U\_Y\_EDS Rev0.7)

(#543611)  
The SATALED# signal is open-collector and requires  
a weak external pull-up (8.2 kΩ to 10 kΩ) to Vcc3.3



(#543016) When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.

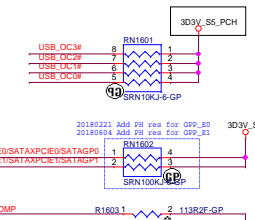


Table 24-3. PCI Express\* Link Configurations Supported

SKL	PCIe Link Config	PCI Express® Lanes											
		1	2	3	4	5	6	7	8	9	10	11	12
U	1x4	Port1				Port5				Port9			
	2x2	Port1	Port3			Port5		Port7		Port9			Port11
	1x2 + 2x1	Port1	Port3	Port4	Port5		Port7	Port8	Port9		Port11	Port12	
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8	Port9	Port10	Port11	Port12
	1x4	Port1				Port5							
Y	2x2	Port1	Port3			Port5		Port7					
	1x2 + 2x1	Port1	Port3	Port4	Port5		Port7	Port8					
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8				
	1x2									Port9			
	2x1									Port9	Port10		

Table 24-2. PCI Express\* Port Feature Details

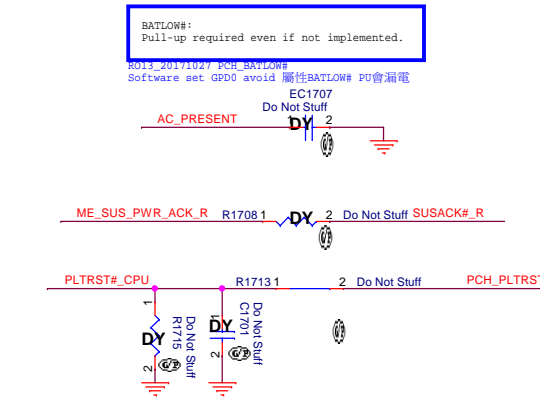
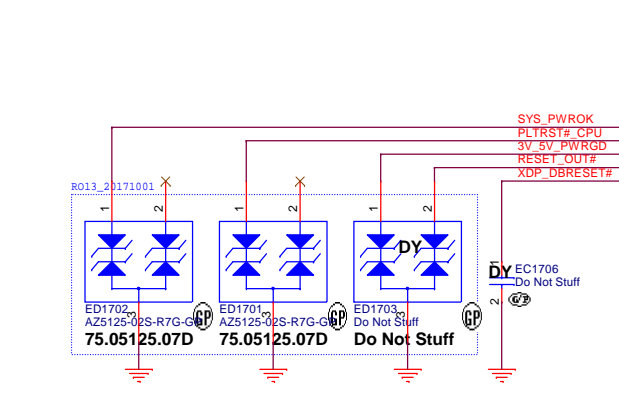
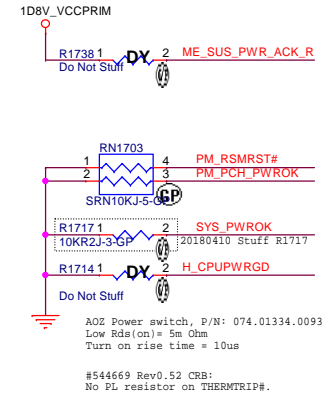
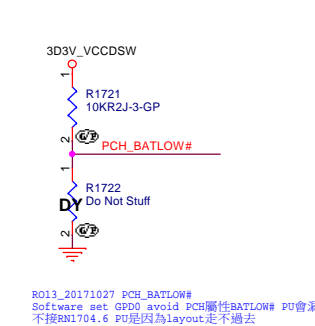
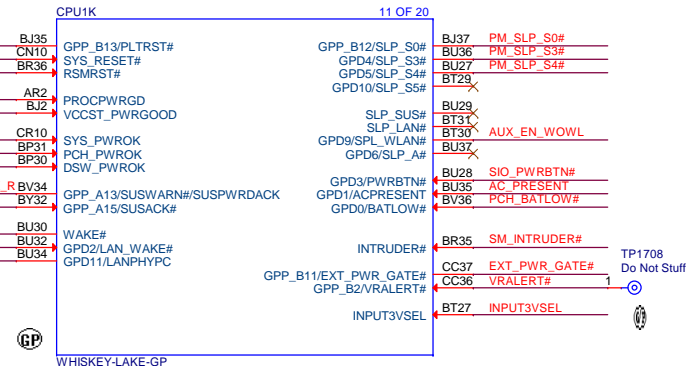
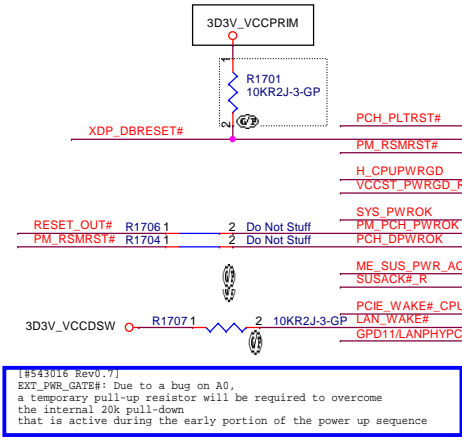
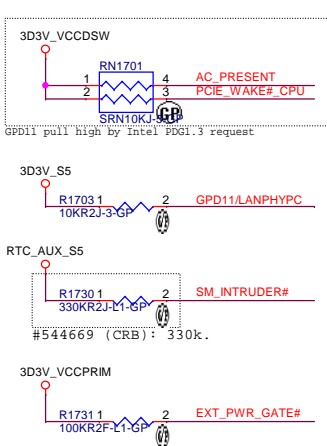
SKL	Max Device (Ports)	Max Lanes	PCIe® Gen Type	Encoding	Transfer Rate (MT/s)	Theoretical Max Bandwidth (GB/s)		
						x1	x2	x4
U	6	12	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00
			3	128b/130b	8000	1.00	2.00	3.94
Y	5	10	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00

«Core Design»



SSID = PCH

- [24] SYS\_PWROK >>>
- [24.26] RESET\_OUT# >>>
- [24.40] VCCST\_PWRGD >>>
- [24] PCH\_RSMRST# >>>
- [25,40,45] 3V\_5V\_PWRGD >>>
- [40,91] PM\_SLP\_S0# <<<
- [40,51] PM\_SLP\_S3# <<<
- [40,53] PM\_SLP\_S4# <<<
- [24,61] AUX\_EN\_WOVL <<<
- [24] SIO\_PWRBTN# >>>
- [43,44] AC\_IN# >>>
- [26,63,66,91] PLTRST#\_CPU <<<
- [3] H\_CPUPWRGD <<<
- [15] INPUT3VSEL >>>

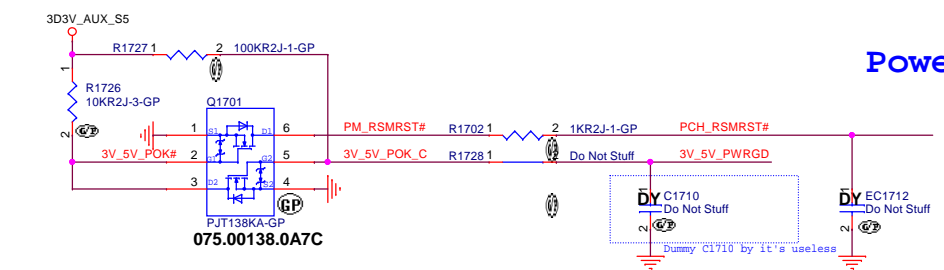


RO13\_20171027 PCH\_BATLOW#  
Software set GPD0 avoid PCH屬性BATLOW# PU會漏電  
不接R1704.6 PU是因為Layout走不過去

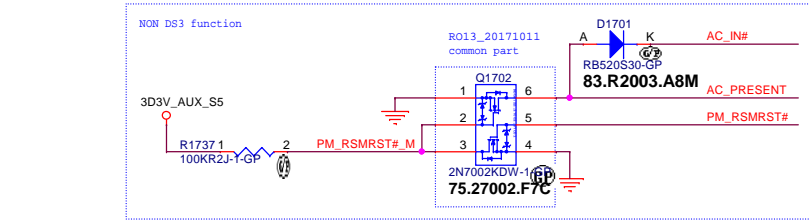
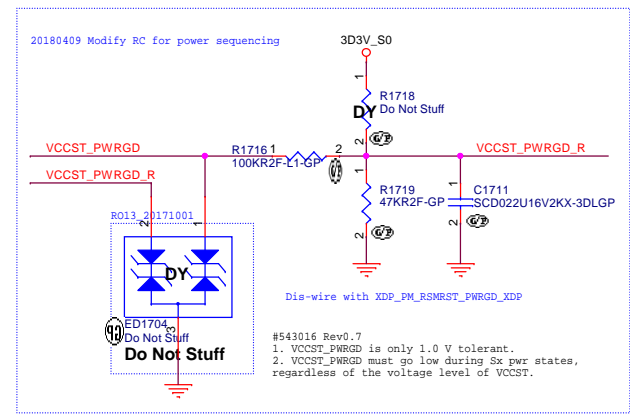
A02 Power switch, P/N: 074.01334.0093  
Low Rds(on) = 5m Ohm  
Turn on rise time = 10us  
#544669 Rev0.52 CRB:  
No PL resistor on THERMTRIP#.

ED1702 AZ5125-02S-R7G-GP 75.05125.07D  
ED1701 AZ5125-02S-R7G-GP 75.05125.07D  
ED1703 Do Not Stuff

AC\_PRESENT  
ME\_SUS\_PWR\_ACK\_R  
PLTRST#\_CPU  
PCH\_PLTRST#



Power Sequence



<Core Design>

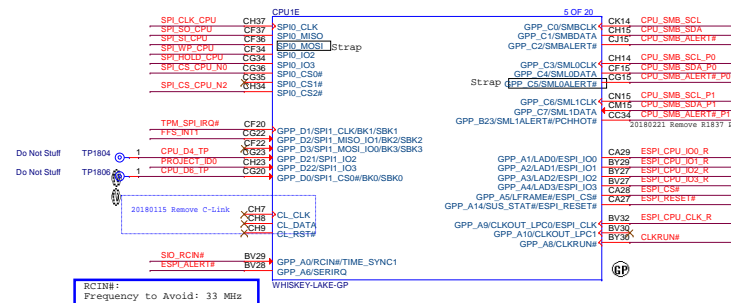
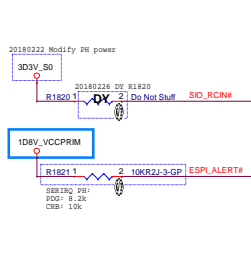
**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title **CPU\_(POWER MANAGEMENT)**

Size A3 Document Number **KR CS MLK 13"** Rev **A00**

Date: Thursday, July 19, 2018 Sheet 17 of 106

[6]	WLAN_CLK_CPU_N	<<<
[6]	WLAN_CLK_CPU_P	<<<
[66]	WLAN_CLKREQ_CPU_N	<<<
[66]	WLAN_CLKREQ_CPU_P	<<<
[63]	SSD_CLK_CPU_N	<<<
[63]	SSD_CLK_CPU_P	<<<
[63]	SSD_CLKREQ_CPU_N	<<<
[25,91]	SPI_SIO_CPU	>>>
[25,91]	SPI_CLK_CPU	<<<
[15,25,91]	SPI_SLCPU	<<<
[25]	SPI_CS_CPU_N0	<<<
[91]	SPI_CS_CPU_N2	<<<
[15,25]	SPI_HOLD_CPU	<<<
[15,25]	SPI_WP_CPU	<<<
[24,68]	ESPI_CPU_IO[3..0]	<<< ESPI_CPU_IO3 ESPI_CPU_IO1 ESPI_CPU_IO0
[24,26]	CPU_SMB_SCL_P1	<<<
[24,26]	CPU_SMB_SDA_P1	<<<
[24,68]	ESPI_CS#	<<<
[24,68]	ESPI_RESET#	<<<
[24,68]	ESPI_CLK	<<<
[24]	SPI_LCU	<<<
[91]	TPM_SPI_IRQ#	<<<
[24,25]	RTCST_ON	>>>
[15]	CPU_SMB_ALERT#	>>>
[15]	CPU_SMB_ALERT#_P0	>>>
[15]	CPU_SMB_ALERT#_P1	>>>
[21]	PROJECT_ID0	>>>
[70]	FFS_INT1	>>>



BOOT HALT	
SPI0_MOSI	0 = ENABLED 1 = DISABLED WEAK INTERNAL PU

This signal has a weak internal pull-up.

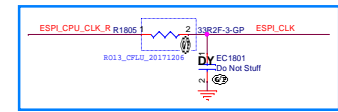
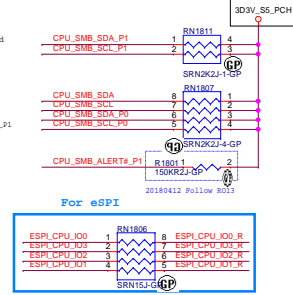
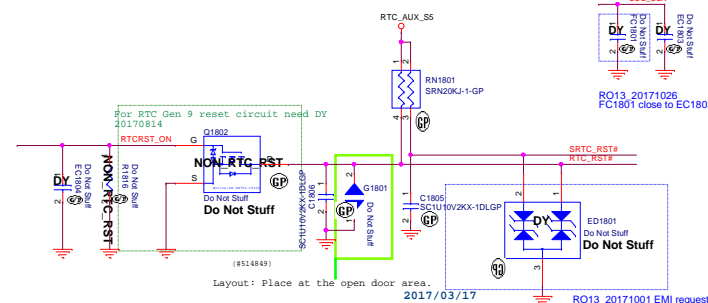
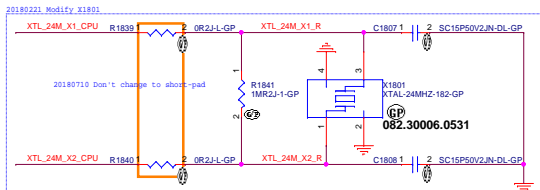
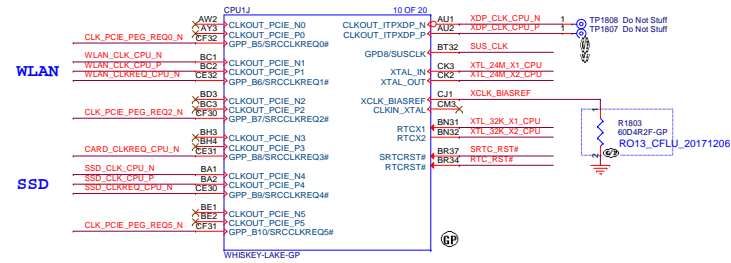
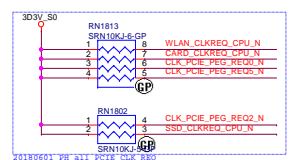
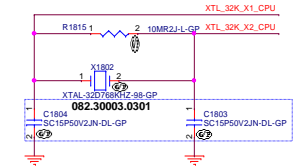


Table 3: Platform Supported Pin Strap Settings for LPC / eSPI / SPI Flash				
ESPI Enable Strap (ESPI_EN) Value (0: LPC, 1: eSPI)	Boot BIOS Strap (BBS) Value (0: SPI, 1: LPC/eSPI)	EC Connection	Boot (BIOS) Flash Connection (Section 3.1.4)	
0	0	LPC	SPI	
0	1	LPC	LPC	
1	0	eSPI	SPI	
1	1	eSPI	eSPI (to EC over eSPI Peripheral Channel) (refer to Section 3.1.4 for details)	

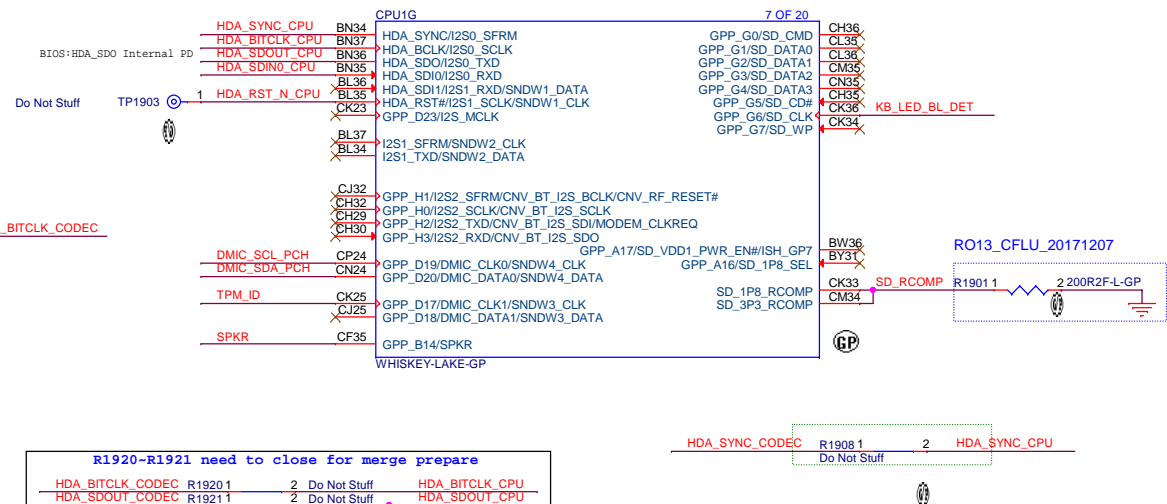
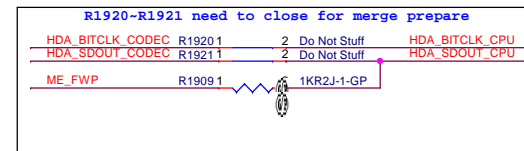
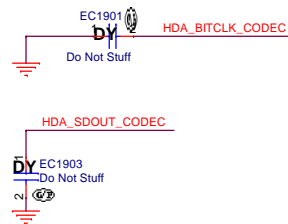
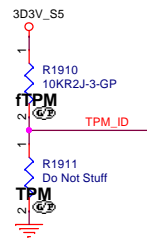
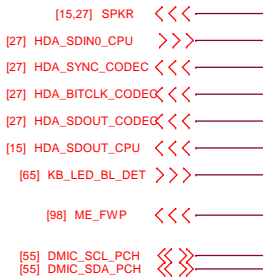
Signal	Logic	When Sampled	Comment
			<p>This Signal has a weak internal Pull-down.</p> <p>This field determines the destination of accesses to the BIOS memory range. Also configurable using Boot BIOS Destination bit (Burst, Device13, Function), offset BCh, bit 6).</p> <div style="text-align: center;"> <pre> graph TD     A[Bit 6] --- B[Boot BIOS Destination SPI (Default)]     B --- C[LPC]             </pre> </div> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>The internal Pull-down is disabled after PLTRST# de-asserts.</li> <li>If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCr's SPI bus with a valid descriptor in order to boot.</li> <li>Boot BIOS Destination select by LPC by functional port or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel IGE or Integrated GBE LAN.</li> <li>This signal is in the primary well.</li> </ol>
GSP1_MOSI/ PRT_B22	Boot BIOS Strap Bit BISS	Rising edge of PCH_PVRK0	<p>This signal has a weak internal Pull-down.</p> <p>= = LPC is selected for EC. (Default) = = eSPI is selected for EC.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>The internal Pull-down is disabled after RSMRST# de-asserts.</li> <li>This signal is in the primary well.</li> </ol>
SMLALERTP/ GPP_C5	eSPI or LPC	Rising edge of RSMRST#	<p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>The internal Pull-down is Disabled after RSMRST# de-asserts.</li> <li>This signal is in the primary well.</li> </ol>



**Strap pin:**

<b>Port B / Port C Detected</b>	Sampled at rising edge of PCH_PWROK
<b>DDPB_CTRLDATA</b>	<p>0 = Port B is not detected.  ★ 1 = Port B is detected.</p>
<b>DDPC_CTRLDATA</b>	<p>0 = Port C is not detected.  ★ 1 = Port C is detected.</p>

These two signals have weak internal pull-down.



RO13\_20171027  
delete ED1901



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Title

### CPU (AUDIO/SDIO/SDXC)

Size

Document Number

**KR CS MLK 13"**

Rev

Date: Thursday, July 19, 2018

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```

[55] CPU_I2C_SDA_P1 >>>>
[55] CPU_I2C_SCL_P1 >>>>

[65] CPU_I2C_SDA_P0 >>>>
[65] CPU_I2C_SCL_P0 >>>>

[55,70] CPU_I2C_SDA_ISH >>>>
[55,70] CPU_I2C_SCL_ISH >>>>

[68] UART_2_CRXD_DTXD >>>>
[68] UART_2_CTXD_DRXD >>>>

[55] GYRO_INT_C >>>>
[55] GYRO_DRDY >>>>

[70] GSEN2_INT1_C >>>>
[70] GSEN2_INT2_C >>>>
[70] FFS_INT2 >>>>

[55] GSEN_INT1 >>>>
[55] GSEN_INT2 >>>>

[15] NRB_BIT >>>>

[15,25] RTC_DET# >>>>

[21] BOARD_ID2 >>>>

[15] CNV_RGL_DT >>>>

[65] KB_DET# >>>>

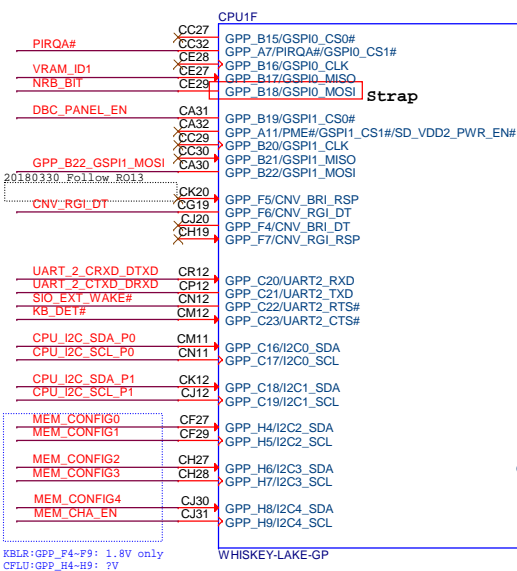
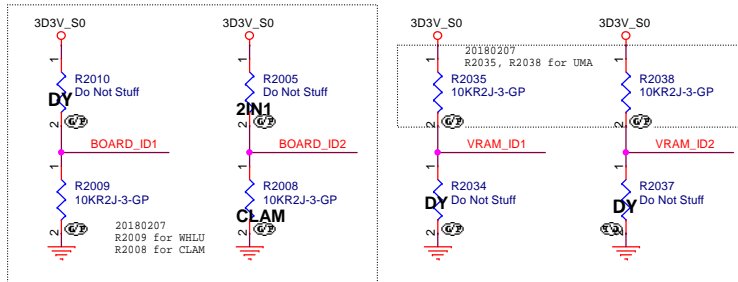
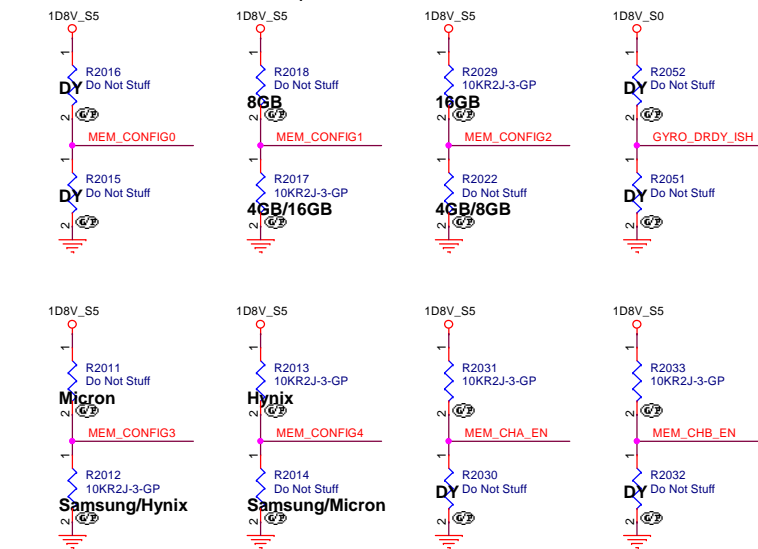
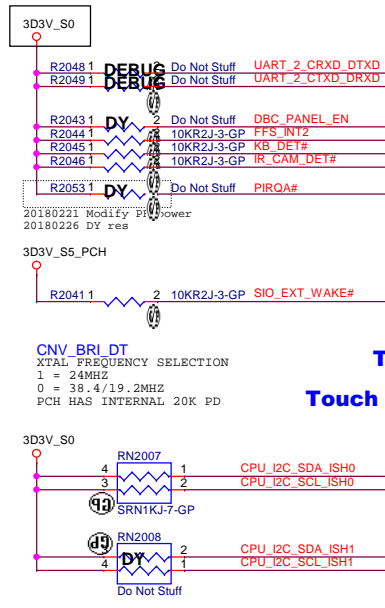
[24] SIO_EXT_WAKE# >>>>

[15] GPP_B22_GSP11_MOSI >>>>

[91] PIRQA# <<<<

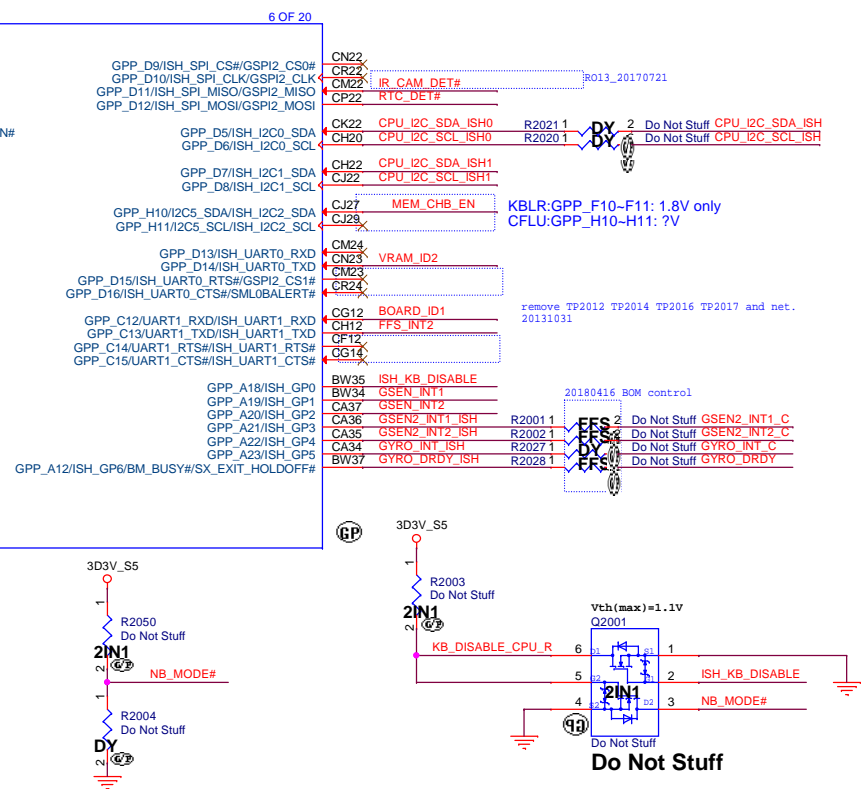
[55] DBC_PANEL_EN <<<<
[55] IR_CAM_DET# <<<<
[24] NB_MODE# <<<<

```



(PDG#543016) Ensure that all I2C interface on-board terminations are pulled up to the same voltage rail as the device/end point.

(PDG#543016) If the UART/GPIO functionality is also not used, the signals can be left as no-connect.



Vender	MEM_CONFIG [0]	MEM_CONFIG[1:2]	MEM_CONFIG[3:4]	Mfr. PN	Wistron PN	Capacity
Samsung	NA	01	00	K4AAG165WB-MCRC	VK98W\$BA	16G
Micron	NA	01	10	MT40A1G16KNR-075E	VK98W\$AB	
Hynix	NA	01	01	H5ANAG6NAMR-UHC	VK98W\$CA	
Samsung	NA	10	00	K4A8G165WB-BCRC	4YVD1\$CA	8G
Micron	NA	10	10	MT40A512M16LY-075E	4YVD1\$BB	
Hynix	NA	10	01	H5AN8G6NAFR-UHC	4YVD1\$AA	
Samsung	NA	00	00	K4A4G165WE-BCRC	M9J68\$BA	4G
Micron	NA	00	10	MT40A256M16GE-083E	M9J68\$AA	
Hynix	NA	00	01	H5AN4G6NBJR-UHC	M9J68\$CA	

VRAM_ID[2:1]	dGPU VRAM size	11	UAM Board
		10	N/A
		01	DIS Board with 4GB VRAM
		00	DIS Board with 2GB VRAM

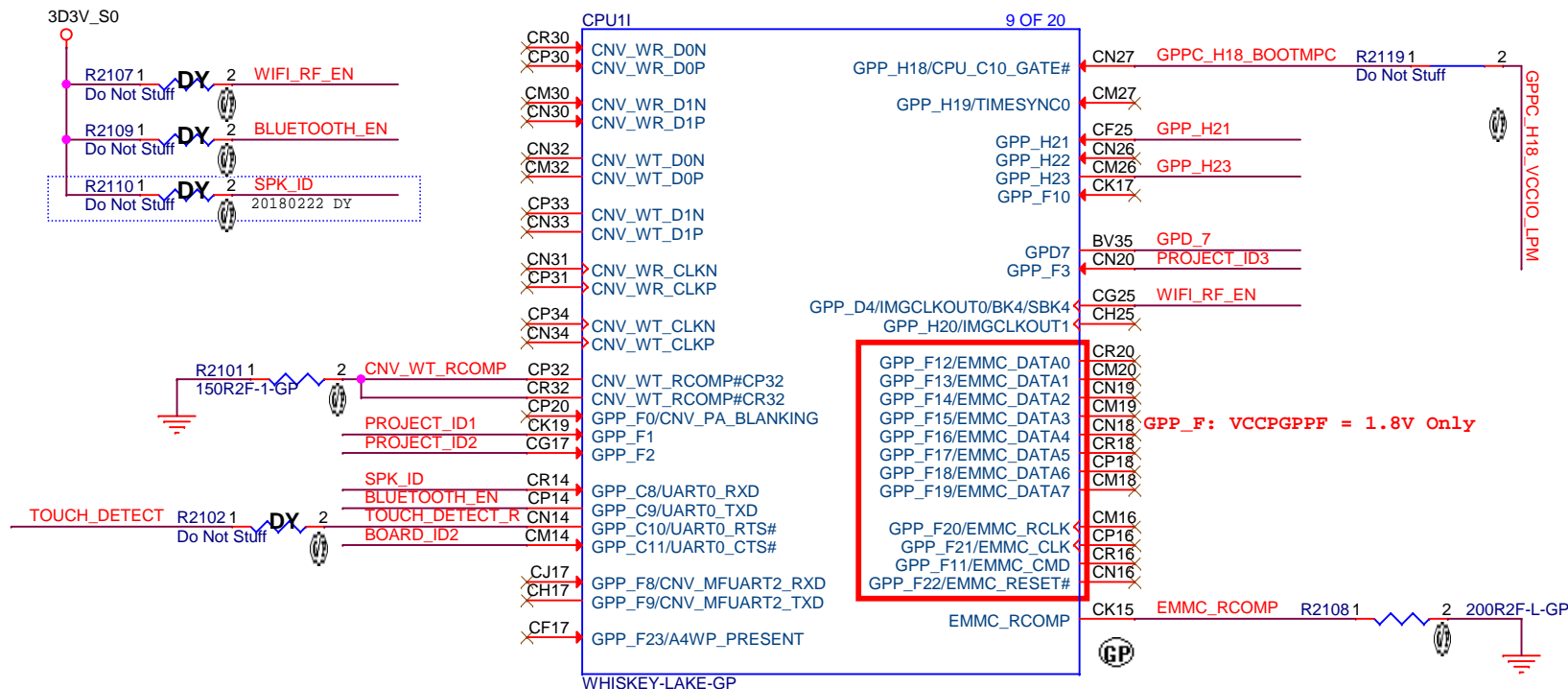


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Title			
<b>CPU (LPSS/ISH)</b>			
Size A3	Document Number		Rev A00
<b>KR CS MLK 13"</b>			
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# SSID = PCH

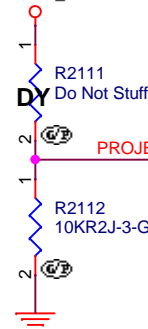
[55] TOUCH\_DETECT >>>  
[66] BLUETOOTH\_EN <<<  
[66] WIFI\_RF\_EN <<<  
[20] BOARD\_ID2 <<<  
[18] PROJECT\_ID0 <<<  
[15] GPP\_H21 >>>  
[15] GPP\_H23 >>>  
[15] GPD\_7 >>>  
[29] SPK\_ID >>>  
[40] GPPC\_H18\_VCCIO\_LPM <<<



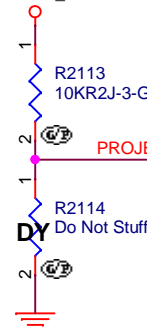
R013\_20171025

## PROJECT\_ID[1:0] 01: 7000 Series

1D8V\_VCCPRIM

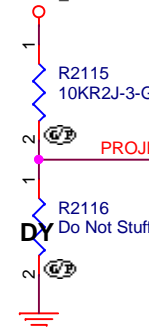


1D8V\_VCCPRIM



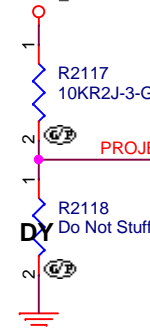
## PROJECT\_ID[3:2]

1D8V\_VCCPRIM



## 11: Inspiron

1D8V\_VCCPRIM



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Title

CPU (POWER1)

Size  
A4

Document Number

KR CS MLK 13"

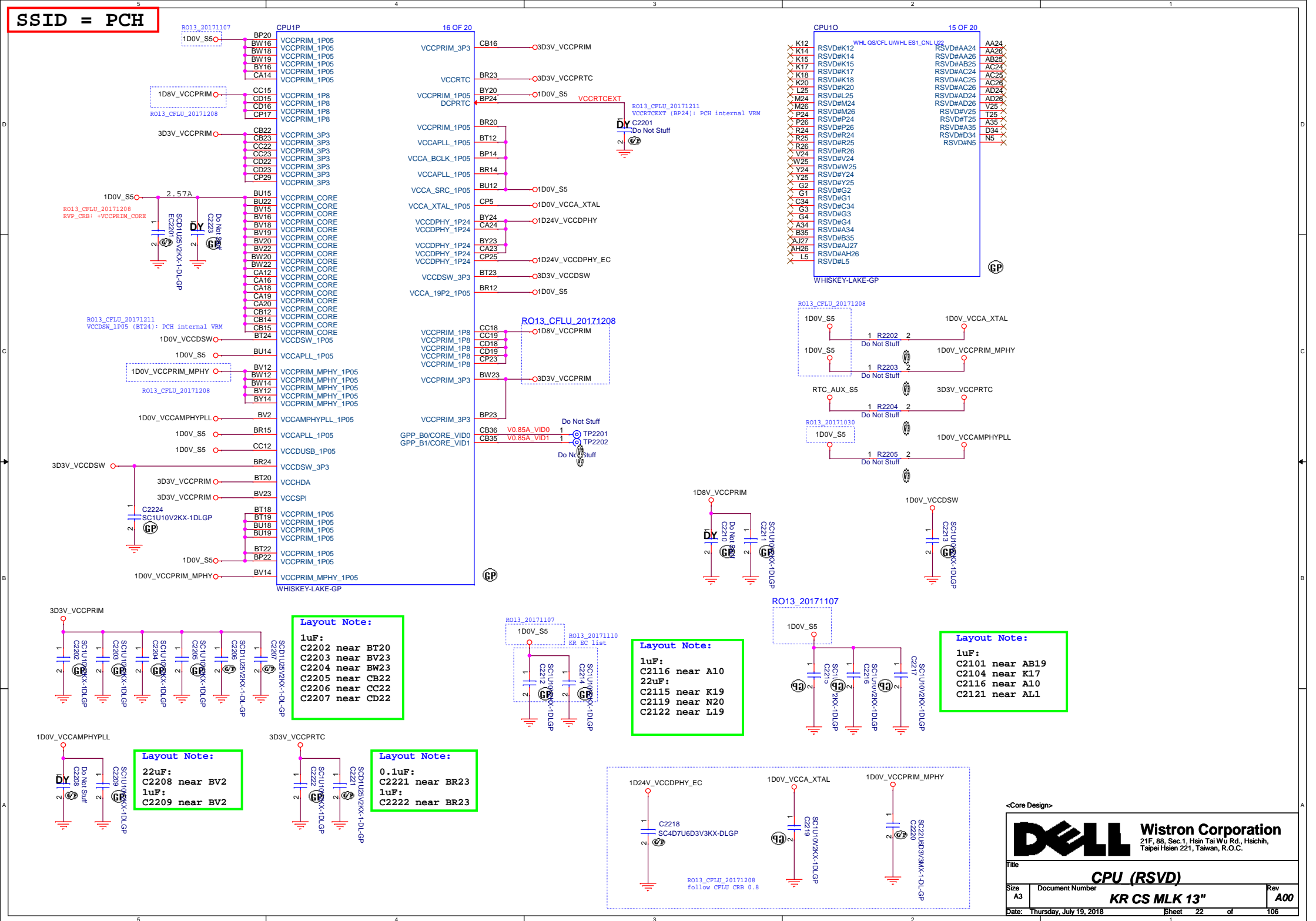
Rev  
A00

Date: Thursday, July 19, 2018

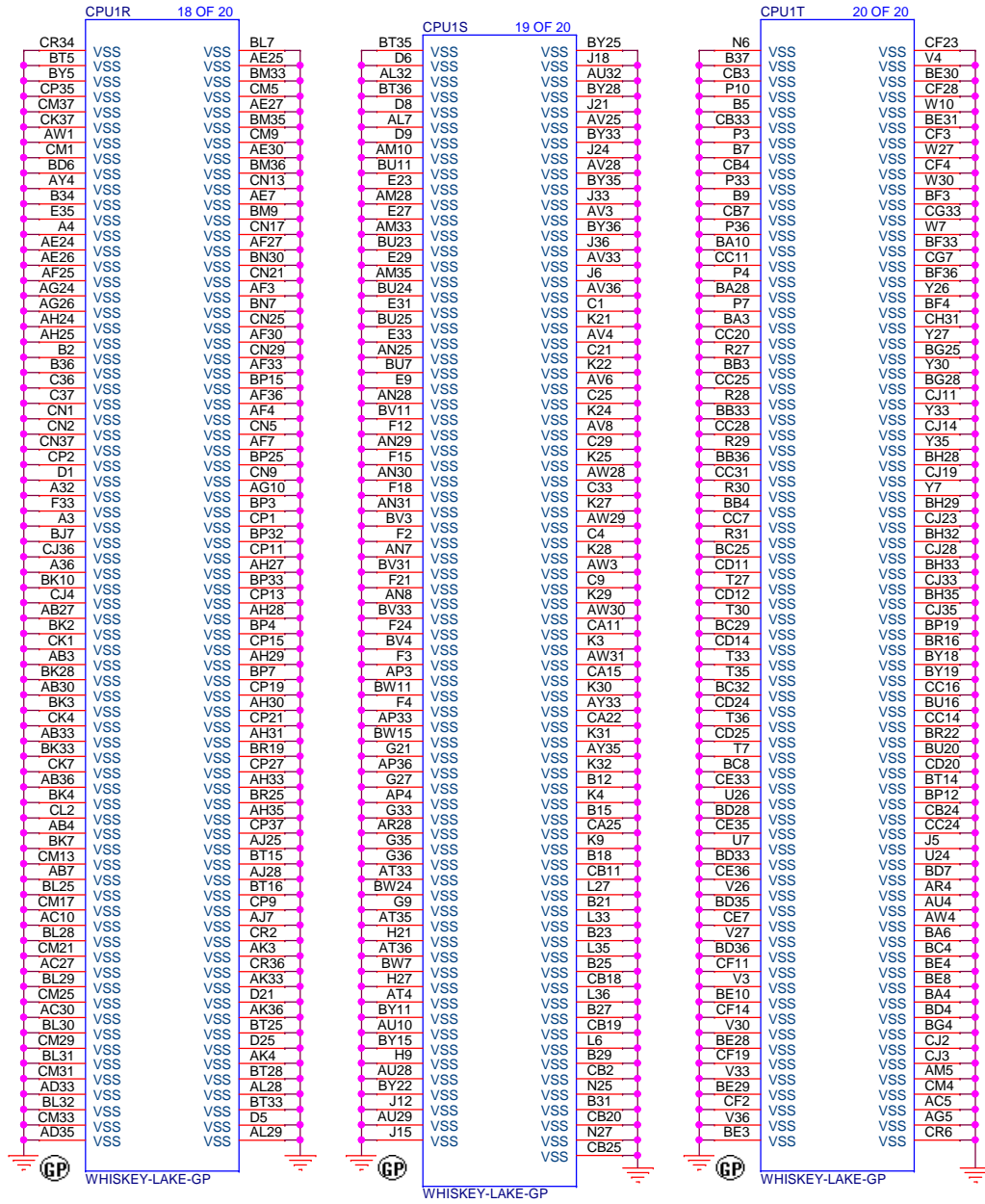
Sheet 21 of 106



**SSID = PCH**







Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	
BA1	NCTFVSS	Test Point (TP)	Corner BB1
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	Corner A1
C1	NCTFVSS	Test Point (TP)	
A5	NCTFVSS	Test Point (TP)	Corner A71
A70	NCTFVSS	Test Point (TP)	
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

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Title		
CPU (VSS)		
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MODEL_ID_DET (GPIO53)	FULL-LOW RESISTOR	FULL-HIGH RESISTOR	VOLTAGE
KR 12" MILA.CMA	100.0K	27.0K(6.27K)2.44K	2.50V
KR 12" MILA.CMA	100.0K	6.65K(0.44K)2.44K	2.80V
KR 12" MILA.DDS	100.0K	15.6K(6.15K)4.05K	1.20V



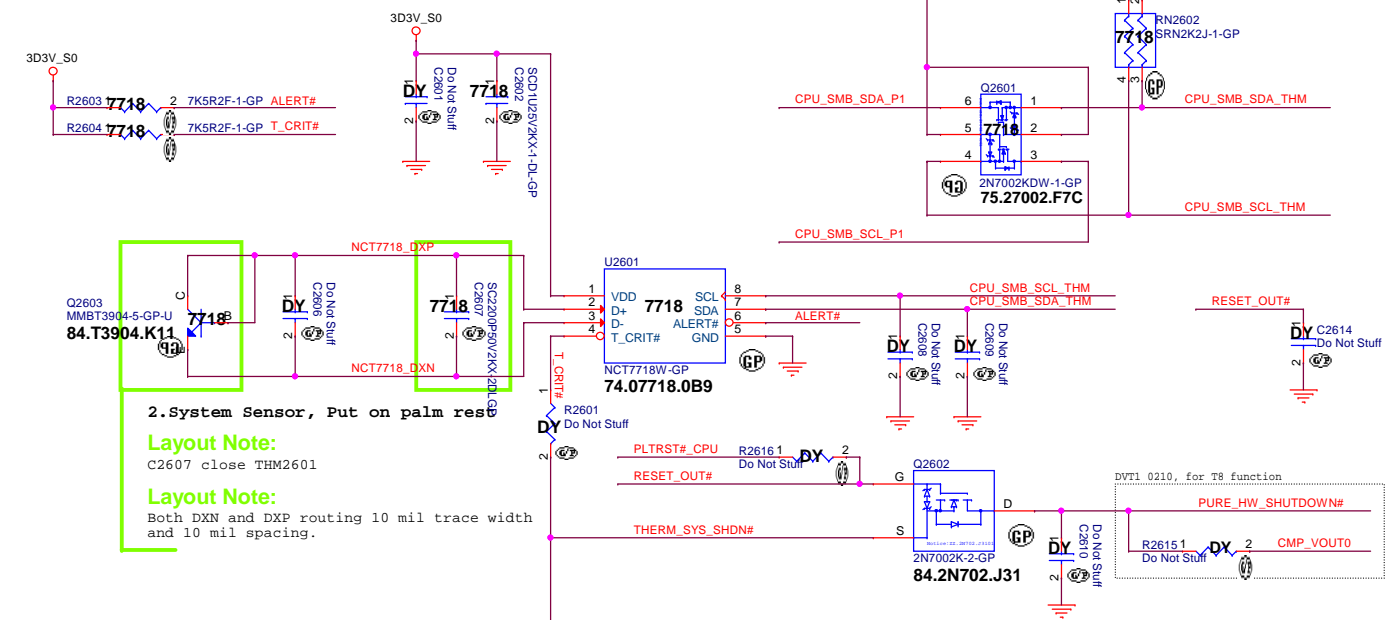
The diagram shows a 12-bit DAC (842N702.J31) and an 8255 PPI. The DAC is connected to a 5V supply and ground. Its output is connected to the CPU's data bus. The PPI is configured as a DAC and is connected to the CPU's data bus and the DAC's output.



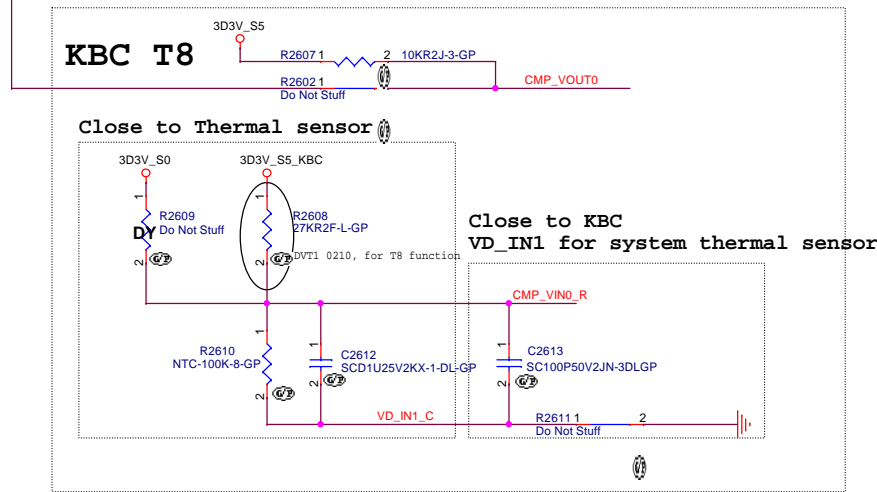
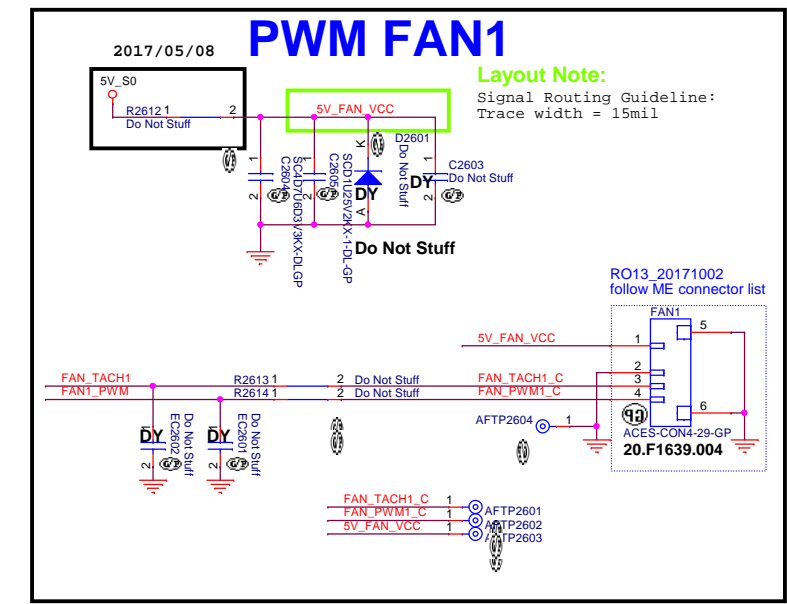
SSID = Thermal Sensor

[18,24] CPU\_SMB\_SDA\_P1 >>>  
[18,24] CPU\_SMB\_SCL\_P1 >>>  
[17,63,66,91] PLTRST#\_CPU >>  
[17,24] RESET\_OUT# >>>  
[24] FAN\_TACH1 <<<  
[24] FAN1\_PWM <<<  
[24] CMP\_VOUT0 <<<  
[24] CMP\_VIN0\_R <<<  
[40] PURE\_HW\_SHUTDOWN# <<<

TEMPERATURE (°C)	T_CRIT#				
	2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107
	7.5KΩ	79	89	99	109
	10.5KΩ	81	91	101	111
	14KΩ	83	93	103	113
	18.7KΩ	85	95	105	115



SSID FAN 07B





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Size	Document Number				Rev
A4	<b>KR CS MLK 13"</b>				<b>A00</b>
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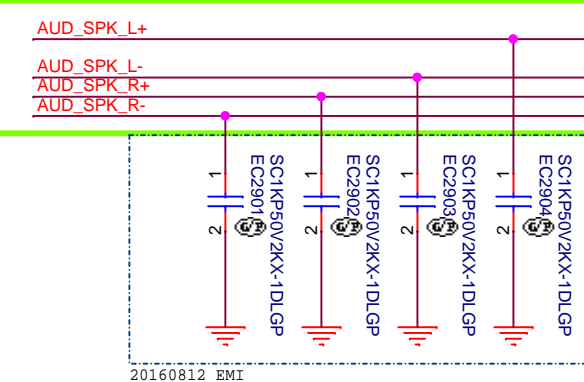
# SSID = Audio

[27] AUD\_SPK\_L+ >>>  
[27] AUD\_SPK\_L- >>>  
[27] AUD\_SPK\_R+ >>>  
[27] AUD\_SPK\_R- >>>  
[27] SPK\_SCL\_CODEC >>>  
[27] SPK\_SDA\_CODEC >>>  
[21] SPK\_ID >>>

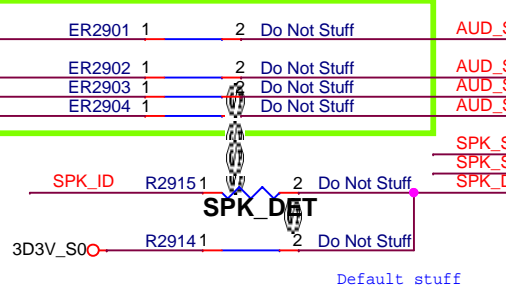
[27] MIC2\_VREFO\_R >>>  
[27] MIC2\_VREFO\_L >>>  
[27] AUD\_RING <<<  
[27] AUD\_HPOUT\_L >>>  
[27] LINE1\_L >>>  
[27] AUD\_HPOUT\_R >>>  
[27] LINE1\_R >>>  
[27] AUD\_SELEEVE <<<  
[27] AUD\_HPJD\_N <<<

## Layout Note:

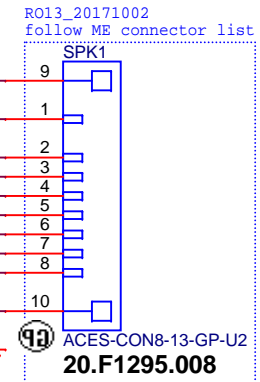
Speaker trace width >40mil @ 2W4ohm speaker power



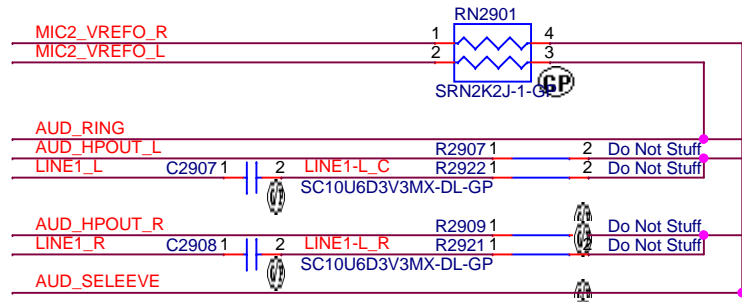
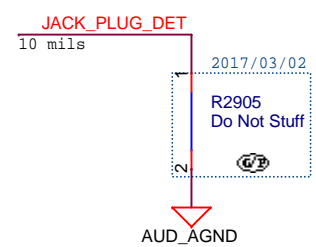
## Speaker



Function	R2914	R2915
EEPROM Speaker	0	NC
Speaker detection	10K	0

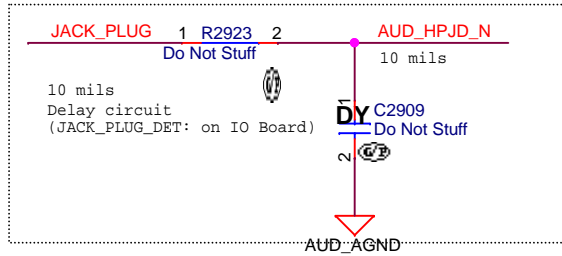
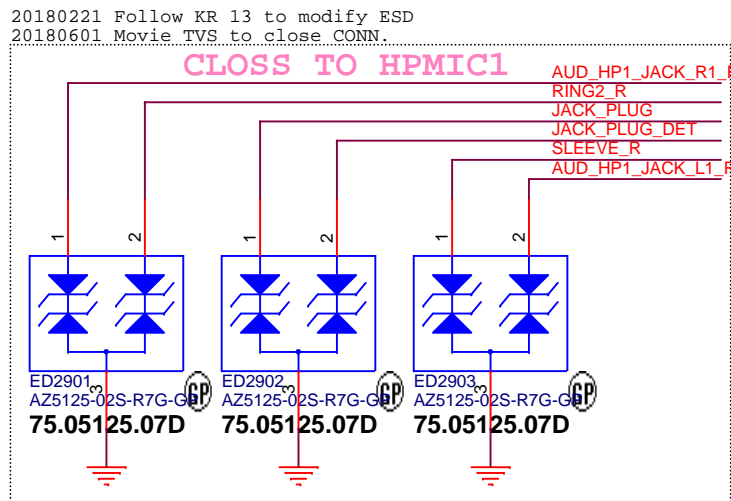
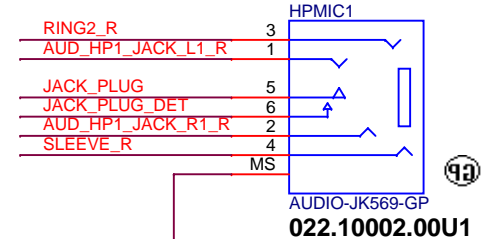
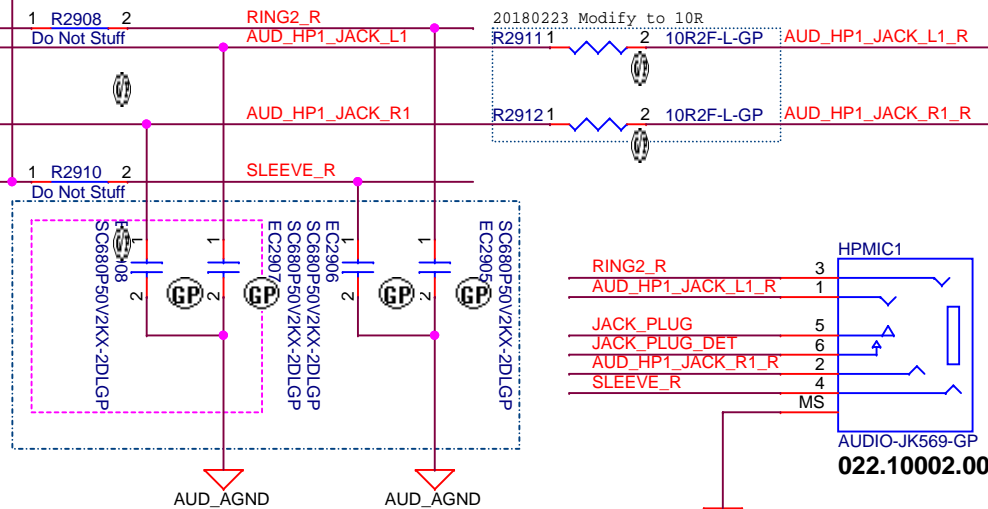


AUD\_SPK\_L- C 1 AFTP2901  
AUD\_SPK\_L+ C 1 AFTP2902  
AUD\_SPK\_R- C 1 AFTP2903  
AUD\_SPK\_R+ C 1 AFTP2904



## Layout Note:

EC2908 EC2907 should place nearby codec IC.



<Core Design>



20160812 EMI

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Title

**Audio IO**

Size A4 Document Number

**KR CS MLK 13"**

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Rev **A00**



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Size A4	Document Number <b>KR CS MLK 13"</b>		Rev <b>A00</b>
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<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>LAN RTL8106</b>		
Size A4	Document Number <b>KR CS MLK 13"</b>	Rev <b>A00</b>
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<Core Design>

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Title			
<b><i>XFOM&amp;RJ45</i></b>			
Size	Document Number		Rev
A4	<b><i>KR CS MLK 13"</i></b>		<b><i>A00</i></b>
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<Core Design>

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Title					
<b>Card Reader-RTS5170</b>					
Size	Document Number				Rev
A4	<b>KR CS MLK 13"</b>				<b>A00</b>
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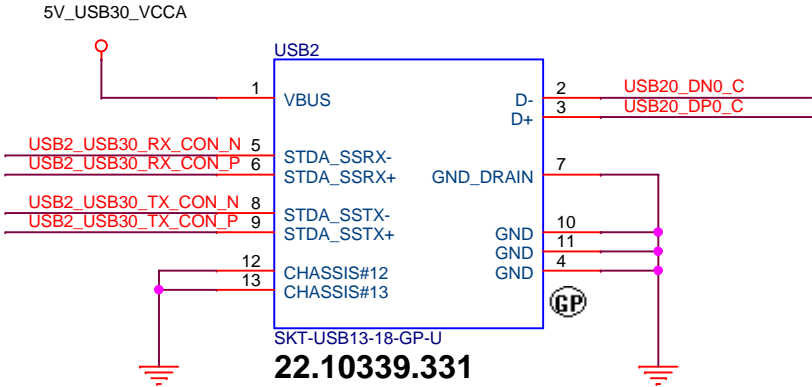
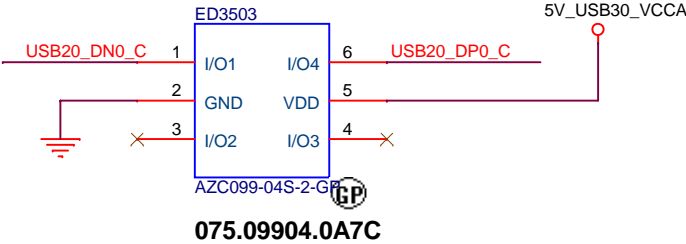
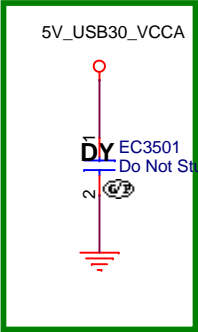
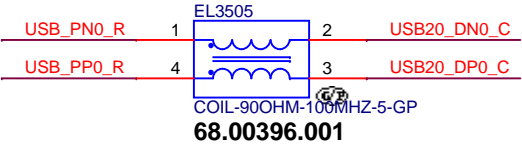
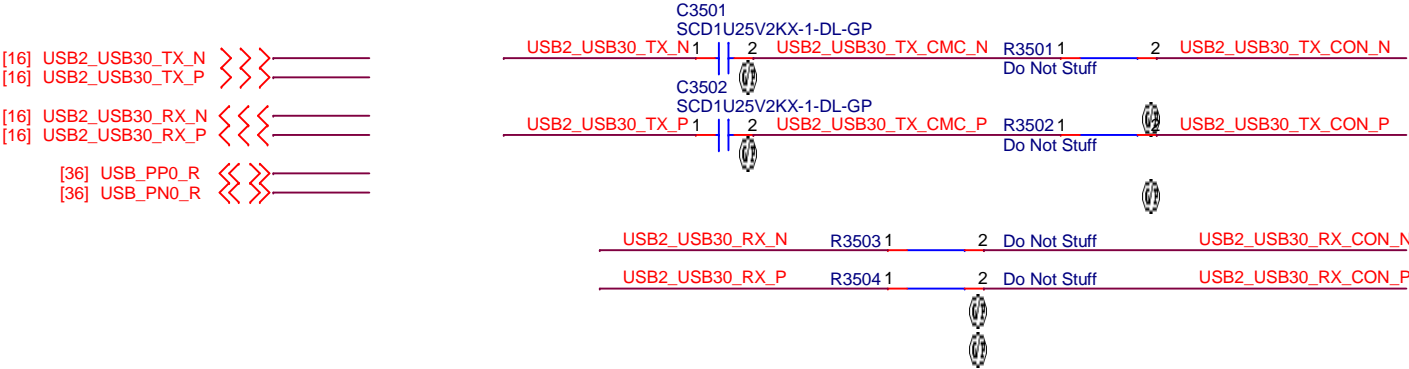
( Blanking )

<Core Design>

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Title <b>(Reserved)</b>					
Size A4	Document Number <b>KR CS MLK 13"</b>				Rev <b>A00</b>
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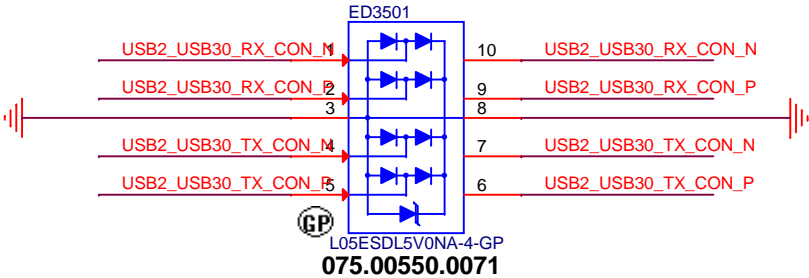
Main Func = USB3.0 Port2

USB3.0 Port2 and USB2.0 Port2



USB 3.0 Connector  
Pin definition

1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	



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Title  
**USB switch**

Size Document Number Rev  
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[35] USB\_PP0\_R <<<>>> \_\_\_\_\_

[35] USB\_PN0\_R <<<>>> \_\_\_\_\_

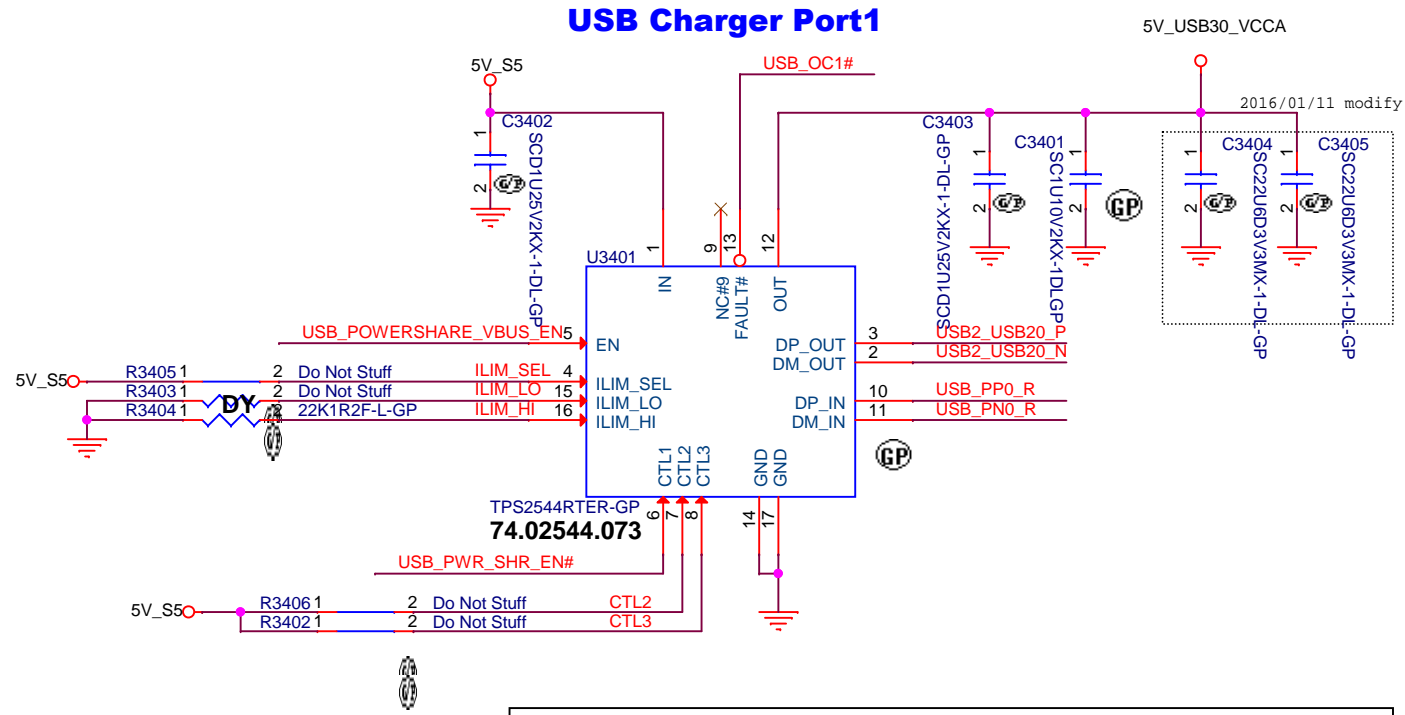
[16] USB2\_USB20\_P <<<>>> \_\_\_\_\_

[16] USB2\_USB20\_N <<<>>> \_\_\_\_\_

[24] USB\_PWR\_SHR\_EN# <<<>>> \_\_\_\_\_

[24] USB\_POWERSHARE\_VBUS\_EN <<<>>> \_\_\_\_\_

[16] USB\_OC1# <<< \_\_\_\_\_



Device Control Pins				
	CTL1 (EC control)	CTL2	CTL3	ILIM_SEL
<b>CDP</b>	<b>1</b>	<b>1</b>	<b>1</b>	<b>1</b>
<b>DCP Auto</b>	<b>0</b>	<b>1</b>	<b>1</b>	<b>X</b>

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Title

**USB30**

Size

A4

Document Number

**KR CS MLK 13"**

Rev

**A00**

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<Core Design>

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Title <b>(Reserved)</b>					
Size A4	Document Number <b>KR CS MLK 13"</b>				Rev <b>A00</b>
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5

4

3

2

1

D

D

C

C

B

B

A

A

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<Core Design>

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Title <b>(Reserved)</b>					
Size A4	Document Number <b>KR CS MLK 13"</b>				Rev <b>A00</b>
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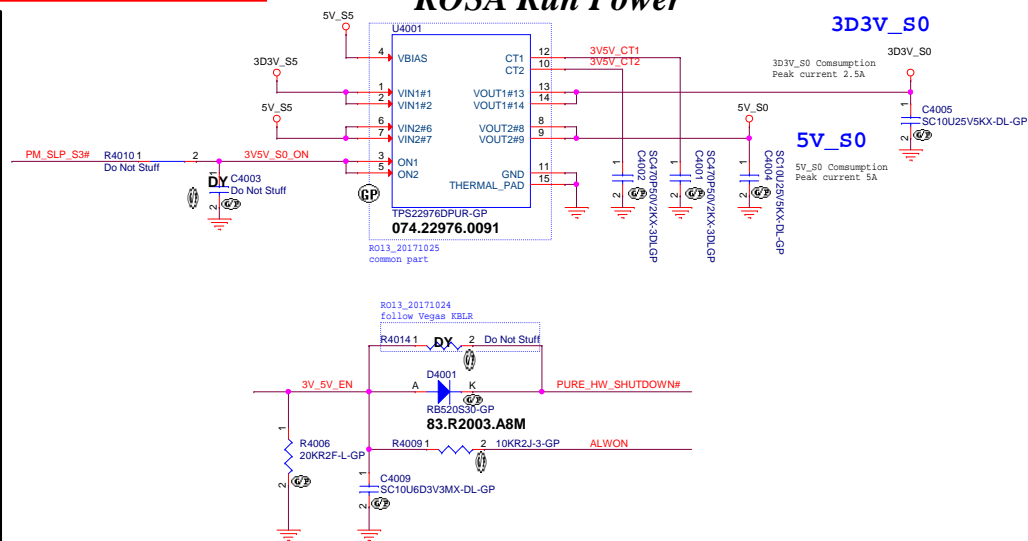
( Blanking )

<Core Design>

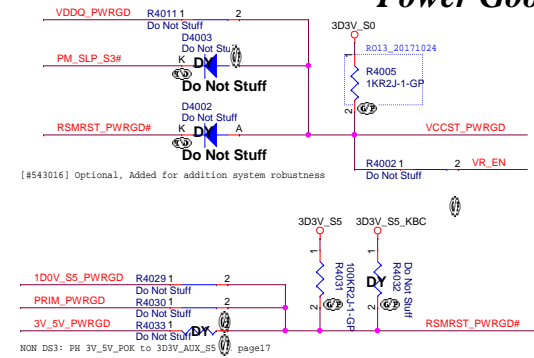
			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>(Reserved)</b>					
Size A4	Document Number <b>KR CS MLK 13"</b>				Rev <b>A00</b>
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### ***ROSA Run Power***

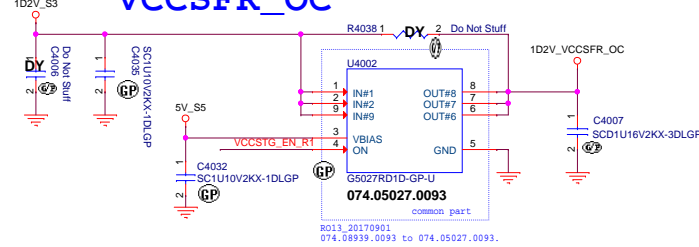
```
[17.53] PM_SLP_S4# >>>
[17.51] PM_SLP_S3# >>>
[17.91] PM_SLP_S0# >>>
[51] VDDO_PWRGD >>>
[24.53] PRIM_PWRGD >>>
[17.25,45] 3V_5V_PWRGD >>>
[52] 1DV0_S5_PWRGD >>>
[24] ALWON >>>
[26] PURE_HW_SHUTDOWN# >>>
[21] GPPC_H18_VCCIO_LPM >>>
```



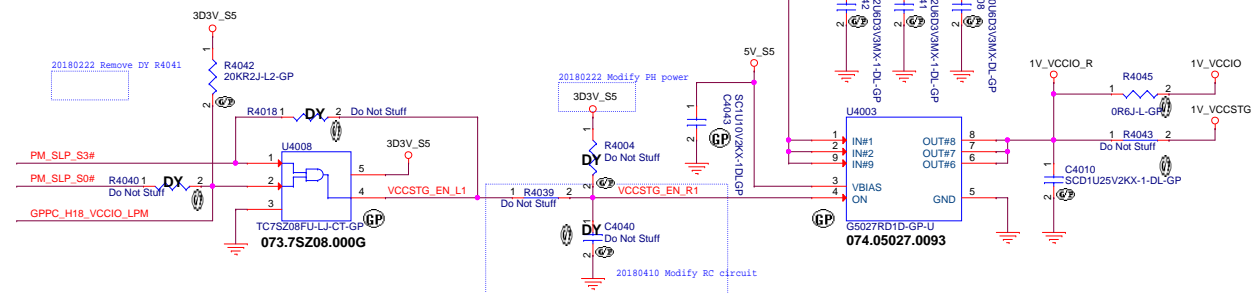
***Power Good***



## VCCSFR\_OC

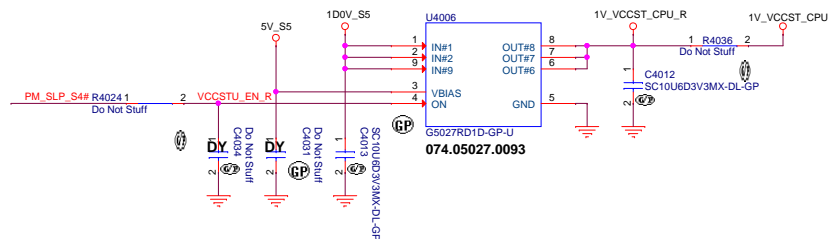


## VCCIO and VCCSTG

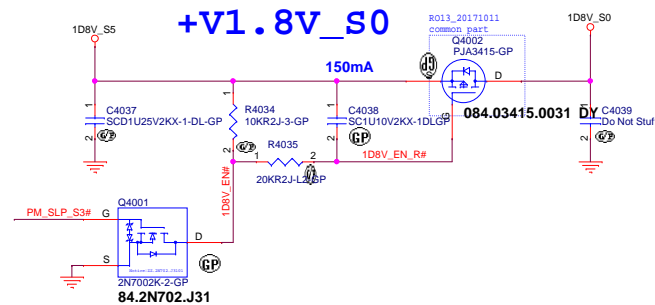


## MANAGEMENT RAIL POWER GENERATION

VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization.



+V1.8V\_S0



**<Core Design>**



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SSID = Power Plane & Sequence

( Blanking )

<Core Design>

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Title <b>Connected_Standby(1/2)+DS3</b>					
Size A4		Document Number <b>KR CS MLK 13"</b>			Rev <b>A00</b>
Date: Thursday, July 19, 2018			Sheet 41 of 106		



( Blanking )

<Core Design>

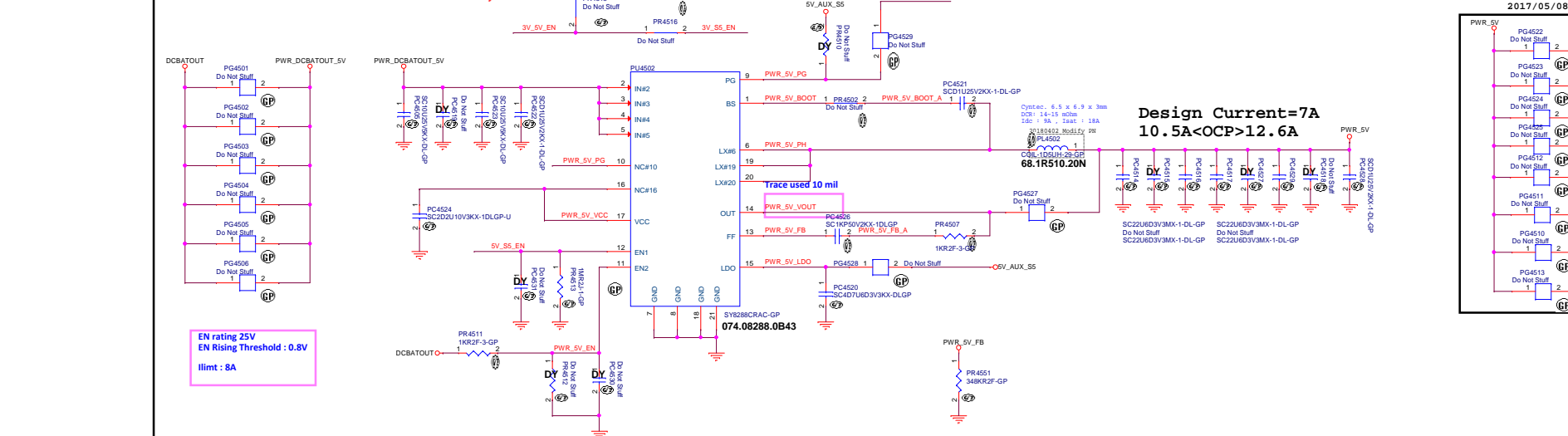
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>Connected_Standby(2/2)</b>		
Size A4	Document Number <b>KR CS MLK 13"</b>	Rev <b>A00</b>
Date: Thursday, July 19, 2018		Sheet 42 of 106



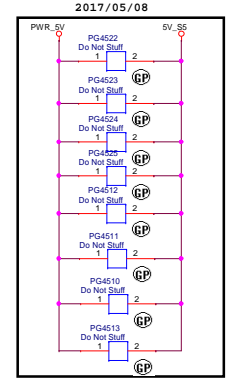


SSID = PWR.Plane.Regulator\_5V

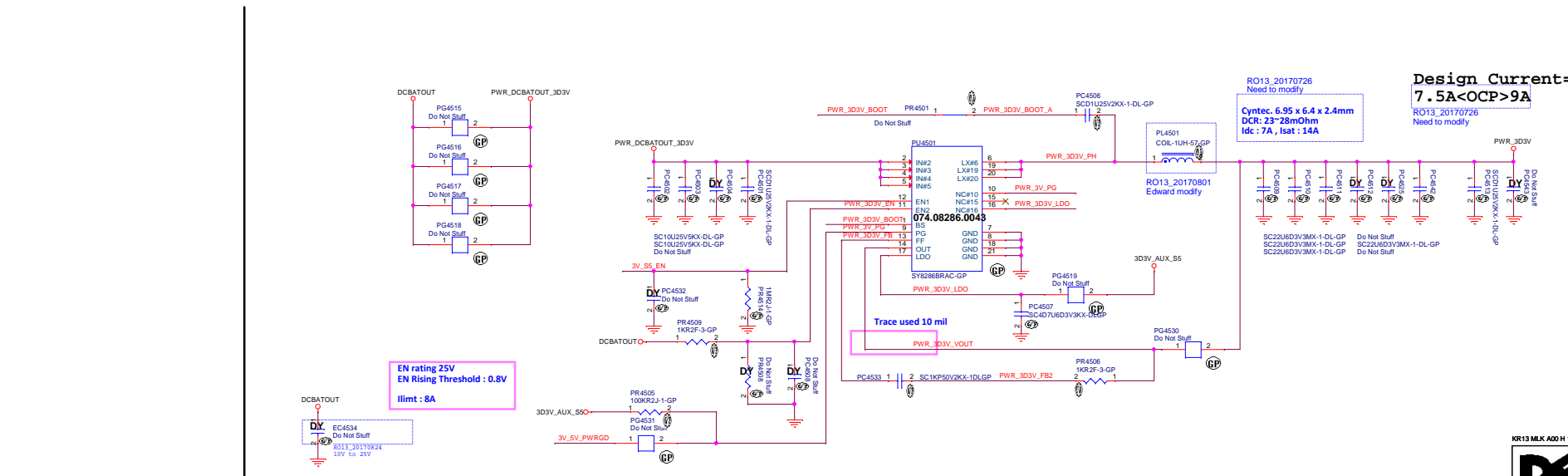
[40] 3V\_5V\_EN >>>  
[17,25,40] 3V\_5V\_PWRGD <<<



EN rating 25V  
EN Rising Threshold : 0.8V  
Ilimt : 8A

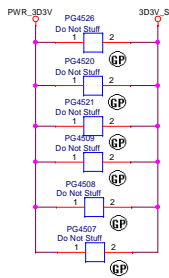


SSID = PWR.Plane.Regulator\_3D3V



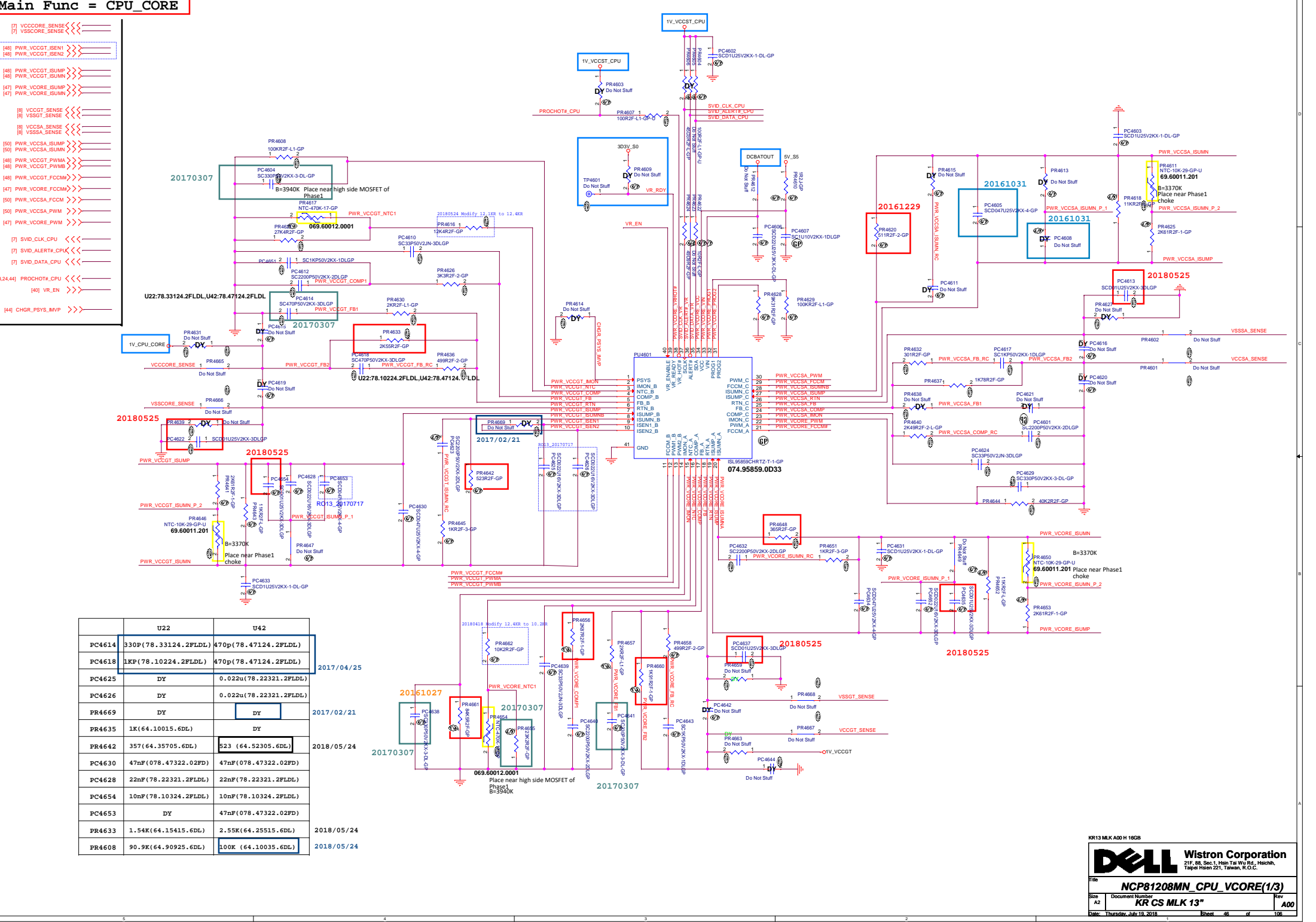
EN rating 25V  
EN Rising Threshold : 0.8V  
Ilimt : 8A

Design Current=8A  
7.5A<OCP>9A



Main Func = CPU\_CORE

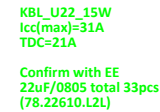
- [7] VCCORE\_SENSE <<<<
- [7] VSSCORE\_SENSE <<<<
- [48] PWR\_VCCGT\_SEN1 <<<<
- [48] PWR\_VCCGT\_SEN2 <<<<
- [48] PWR\_VCCGT\_ISUMP <<<<
- [48] PWR\_VCCGT\_ISUMN <<<<
- [47] PWR\_VCORE\_ISUMP <<<<
- [47] PWR\_VCORE\_ISUMN <<<<
- [8] VCCGT\_SENSE <<<<
- [8] VSSGT\_SENSE <<<<
- [8] VCCSA\_SENSE <<<<
- [8] VSSSA\_SENSE <<<<
- [50] PWR\_VCCSA\_ISUMP <<<<
- [50] PWR\_VCCSA\_ISUMN <<<<
- [48] PWR\_VCCGT\_PWM <<<<
- [48] PWR\_VCCGT\_PWMB <<<<
- [48] PWR\_VCORE\_FCOM <<<<
- [50] PWR\_VCCSA\_FCOM <<<<
- [47] PWR\_VCORE\_PWM <<<<
- [7] SVID\_CLK\_CPU <<<<
- [7] SVID\_ALERTN\_CPU <<<<
- [7] SVID\_DATA\_CPU <<<<
- [3,24,44] PROCHOTN\_CPU <<<<
- [40] VR\_EN <<<<
- [4] CHGR\_PSVS\_MVP <<<<



	U22	U42
PC4614	330P(78.33124.2FLDL)	470p(78.47124.2FLDL)
PC4618	1K(78.10224.2FLDL)	470p(78.47124.2FLDL)
PC4625	DY	0.022u(78.22321.2FLDL)
PC4626	DY	0.022u(78.22321.2FLDL)
PC4669	DY	DY
PC4635	1K(64.10015.6DL)	DY
PC4642	357(64.35705.6DL)	523(64.52305.6DL)
PC4630	47nF(078.47322.02FD)	47nF(078.47322.02FD)
PC4628	22nF(78.22321.2FLDL)	22nF(78.22321.2FLDL)
PC4654	10nF(78.10324.2FLDL)	10nF(78.10324.2FLDL)
PC4653	DY	47nF(078.47322.02FD)
PC4633	1.54K(64.15415.6DL)	2.55K(64.25515.6DL)
PC4608	90.9K(64.90925.6DL)	100K(64.10035.6DL)

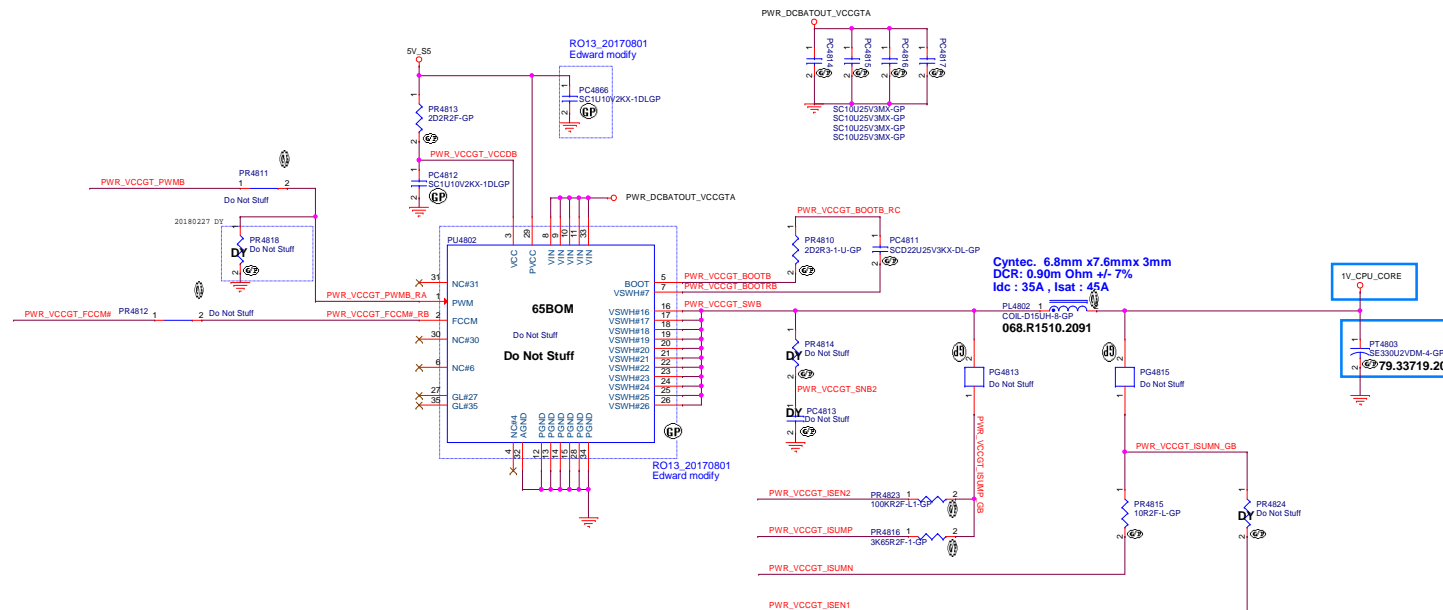
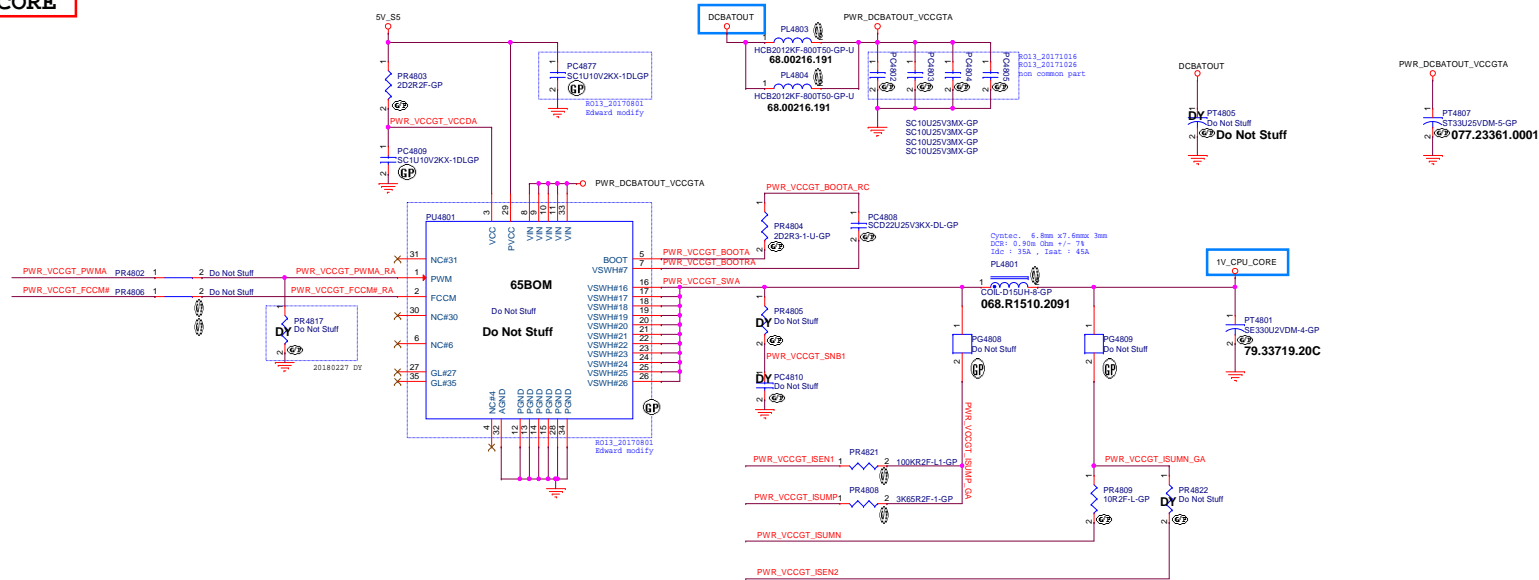
```
[46] PWR_VCORE_PWM      >>>
[46] PWR_VCORE_FCCM#     >>>

[46] PWR_VCORE_ISUMP      <<<
[46] PWR_VCORE_ISUMN      <<<
```





```
Main Func = CPU_CORE
```




KBL-R\_U42\_15W  
Icc(max)=64A  
TDC=42A

Confirm with EE  
22uF/0805 total 36pcs  
(78.22610.L2L)

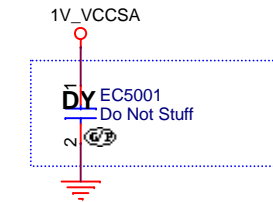
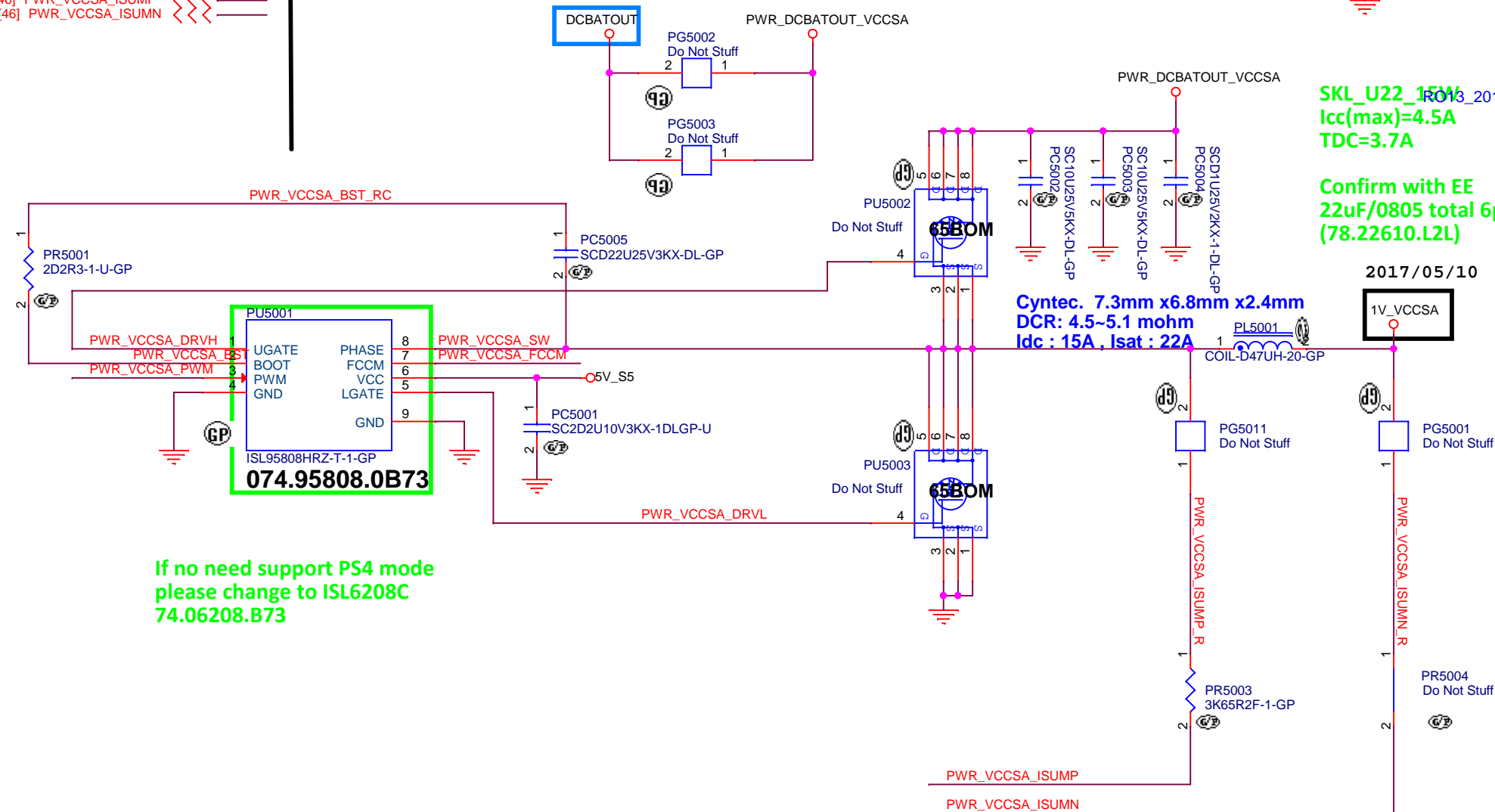
( Blanking )

KR13 MLK A00 H 16GB

			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>NCP81210MN_CPU_VCCGTUS</b>					
Size A4		Document Number <b>KR CS MLK 13"</b>			Rev <b>A00</b>
Date: Thursday, July 19, 2018			Sheet 49 of 106		

SSID = CPU\_CORE

[46] PWR\_VCCSA\_PWM  
[46] PWR\_VCCSA\_FCCM  
[46] PWR\_VCCSA\_ISUMP  
[46] PWR\_VCCSA\_ISUMN



SKL\_U22\_15W  
Icc(max)=4.5A  
TDC=3.7A

Confirm with EE  
22uF/0805 total 6pcs  
(78.22610.L2L)

2017/05/10

If no need support PS4 mode  
please change to ISL6208C  
74.06208.B73

KR13 MLK A00 H 16GB

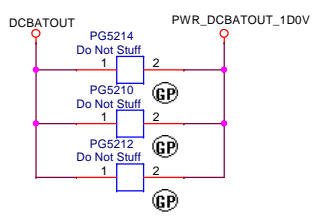


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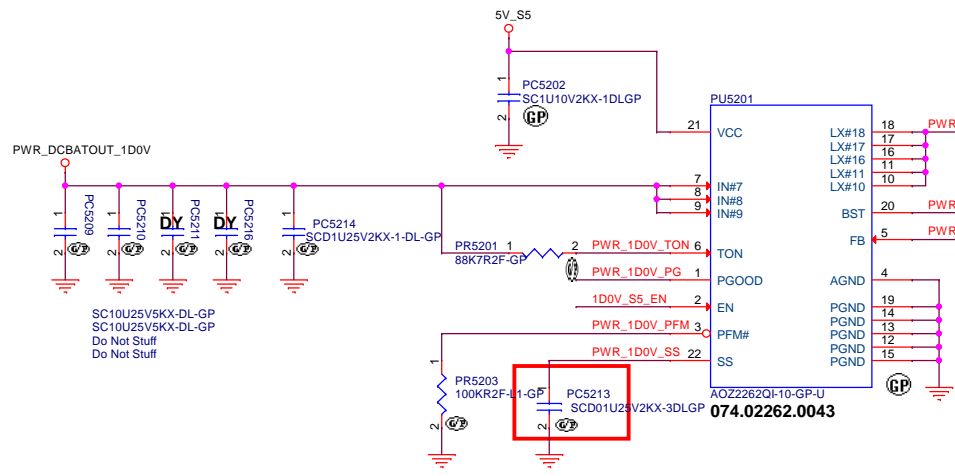
Title			VCCSA	
Size	Document Number		Rev	
A4	KR CS MLK 13"		A00	
Date: Thursday, July 19, 2018		Sheet 50 of 106		



[40] 1D0V\_S5\_PWRGD <<<  
[25,53] 3V\_5V\_DSW\_OK >>>



# AOZ2262 for 1D0V

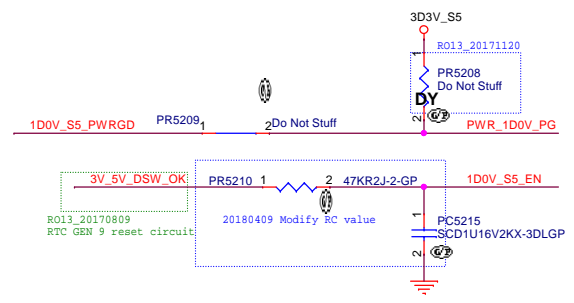
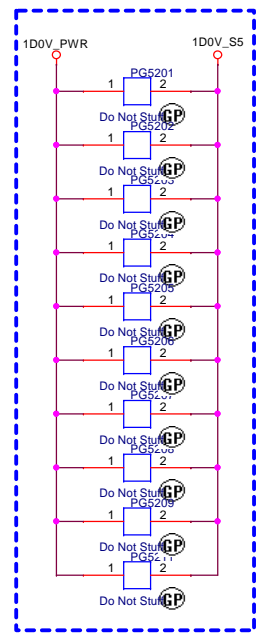


Cyntec 6.8\*7.3\*2.4  
DCR: 11.2m-13.5 mOhm  
Ide : 9 A , Isat : 16A  
2018/02/9 change

Design Current : 9A  
11.25A<OCP>13.5A

$$V_o = 0.8 \times (1 + R1/R2) = 0.8 \times (1 + 3.16/10) = 1.0528V$$

2016/12/16



20180525

KR13 MLK A00 H 16GB



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Title <b>(Reserved)</b>		
Size A3	Document Number <b>KR CS MLK 13"</b>	Rev <b>A00</b>
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SSID = 2D5V/ 1D8V

[15,21] 2D5V\_S3\_PWRGD <<< \_\_\_\_\_  
[17,40] PM\_SLP\_S4# >>> \_\_\_\_\_

[24,40] PRIM\_PWRGD <<< \_\_\_\_\_  
[25,52] 3V\_5V\_DSW\_OK >>> \_\_\_\_\_

2D5V\_S3\_PWRGD  
PM\_SLP\_S4#

```

RO13_20170809
RTC GEN 9 reset circuit

```

KR13 MLK A00 H 16GB



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Title

**(Reserved)**

Size  
A4

Document Number

**KR CS MLK 13"**

Rev

**A00**

Date: Thursday, July 19, 2018

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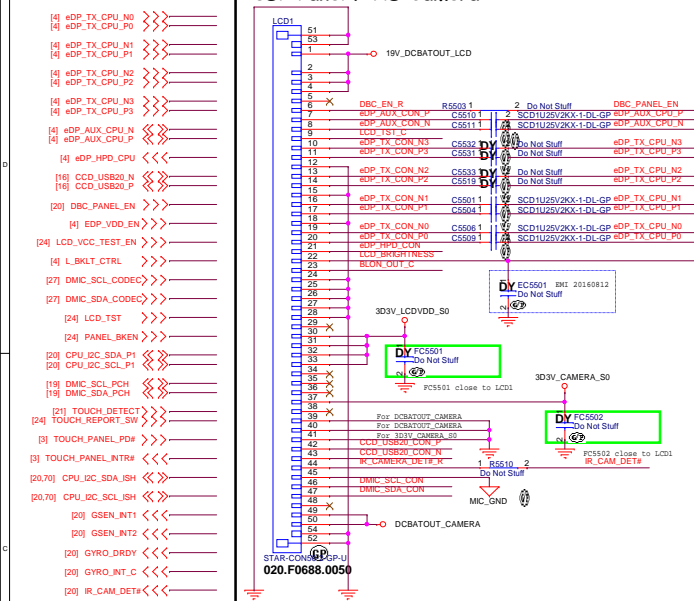


( Blanking )

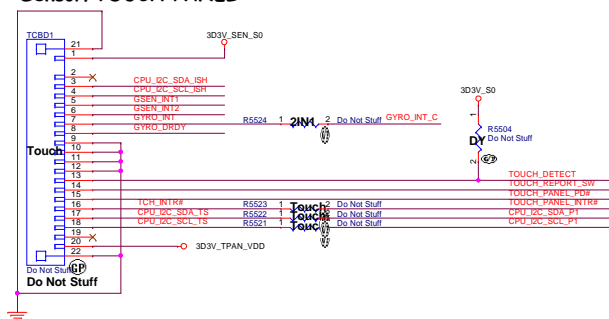
<Core Design>

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Title <b>(Reserved)</b>					
Size A4	Document Number <b>KR CS MLK 13"</b>				Rev <b>A00</b>
Date: Thursday, July 19, 2018		Sheet 54		of 106	

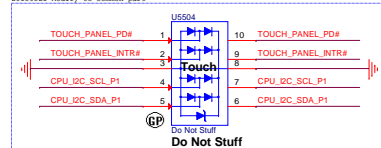
**eDP Panel / HD Camera**



### Sensor/TOUCH PANEL



20180521 Modify to common part.

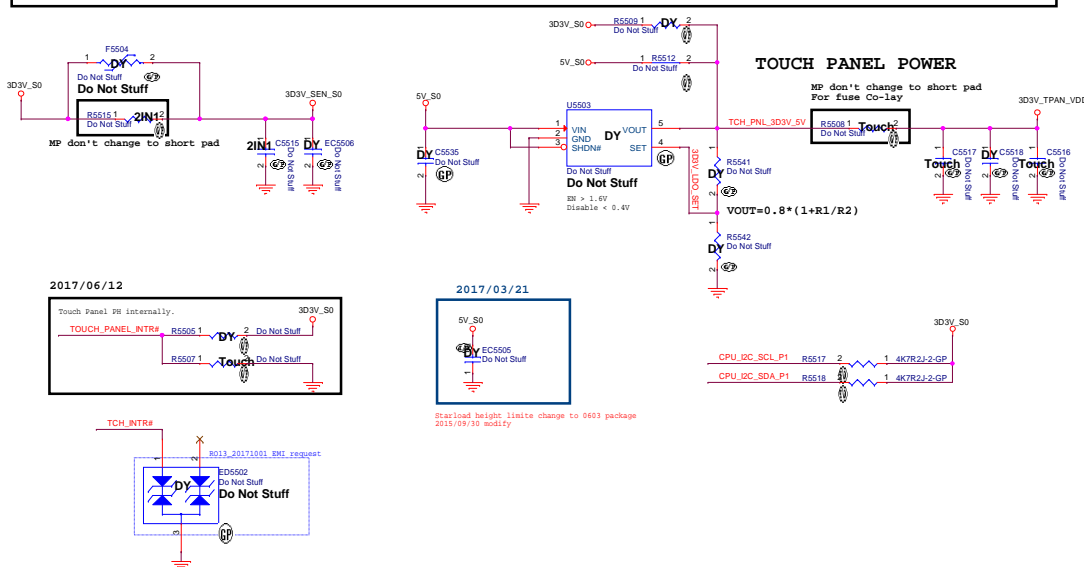
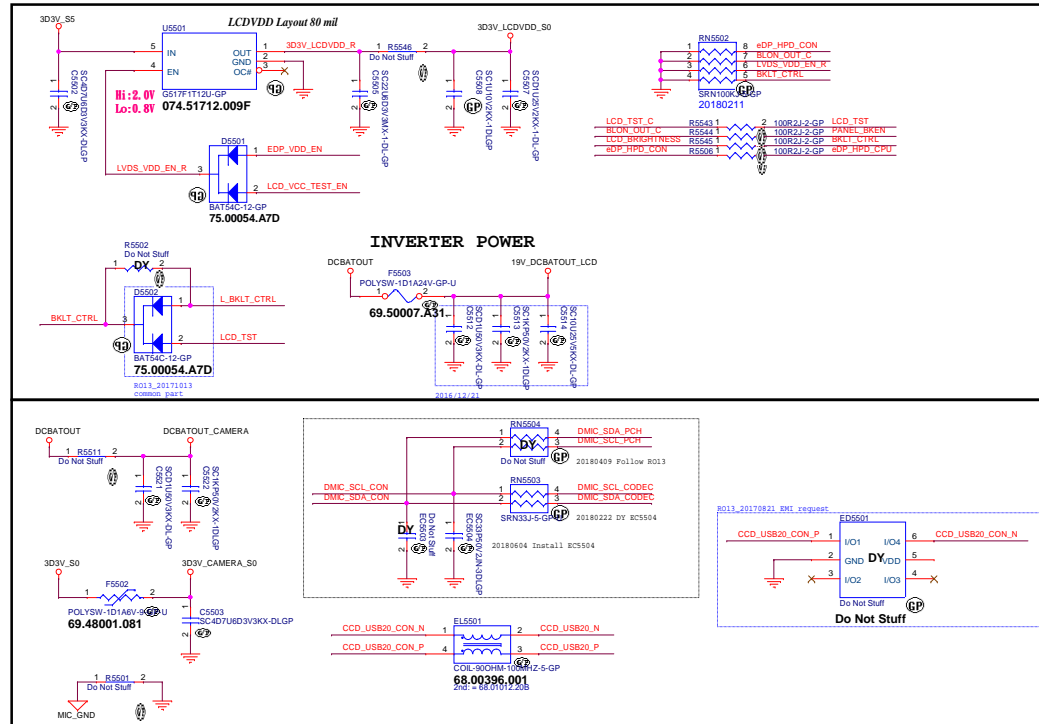


6315 TP 小燈上有預留以下訊號 pull-high  
Thank!

IO Pull-High



Best Regards  
William Hsu



«Core Design:



Title **LCD&CAM&DMC&Touch**

Size A2	Document Number <b>KR CS MLK 13"</b>	Rev <b>A00</b>
Date: Thursday, July 19, 2018	Sheet 55 of 106	

(Blanking)

<Core Design>

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Title <b>CRT</b>			
Size A4	Document Number <b>KR CS MLK 13"</b>		Rev <b>A00</b>
Date: Thursday, July 19, 2018		Sheet 56 of	106

102V\_HDMI\_EN

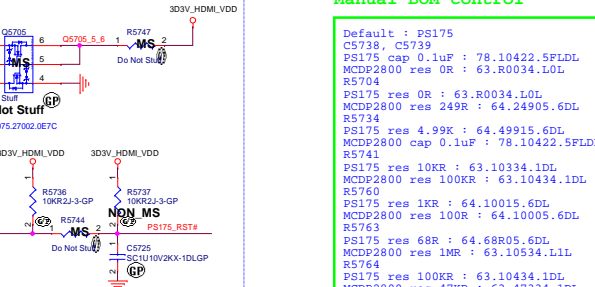
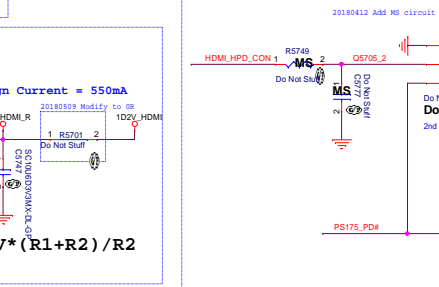
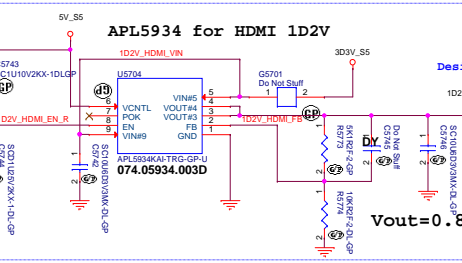
Do Not Sulf

R5775

P0175 res GR : 63.80234.LOL

MCPD2800 res 10ER : 63.10334.LOL

20180409 Follow B013



```

Default: PS175
CS738, CS739
PS175 cap 0.1uF : 78.10422.5FLDL
MCDP2800 res OR : 63.R0034.L0L
R5704
PS175 res OR : 63.R0034.L0L
MCDP2800 res 249R : 64.24905.6DL
R5734
PS175 res 4.9K : 64.49915.6DL
MCDP2800 cap 0.1uF : 78.10422.5FLDL
R5741
PS175 res 10KR : 63.10334.1DL
MCDP2800 res 100KR : 63.10434.1DL
R5760
PS175 res 1KR : 64.10015.6DL
MCDP2800 res 100R : 64.10005.6DL
R5763
PS175 res 68R : 64.68005.6DL
MCDP2800 res 1MR : 63.10534.L1L
R5764
PS175 res 100KR : 63.10434.1DL
MCDP2800 res 47KR : 63.47334.1DL
R5775
PS175 res OR : 63.R0034.L0L
MCDP2800 res 10KR : 63.10334.1DL
U5701
PS175 : 071.17564.000U
MCDP2800 : 071.02800.0A0U
U5702
PS175 : 72.25200.001
MCDP2800 : 072.25080.0001

```

( Blanking )

<Core Design>

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Date: Thursday, July 19, 2018			Sheet 58 of 106		

(Blanking)

<Core Design>

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Size A4		Document Number <b>KR CS MLK 13"</b>			Rev
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( Blanking )

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***SATA IF HDD/ODD***

Size  
A4

Document Number

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[17,24] AUX\_EN\_WOWL>>>\_\_\_\_\_

**NGFF\_WLAN\_CONN**

Rev

**KR CS MLK 13"**

**A00**

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( Blanking )

<Core Design>

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Title					
<b>Reserved</b>					
Size	Document Number				Rev
A4	<b>KR CS MLK 13"</b>				<b>A00</b>
Date: Thursday, July 19, 2018			Sheet	62	of 106

SSID = M.2

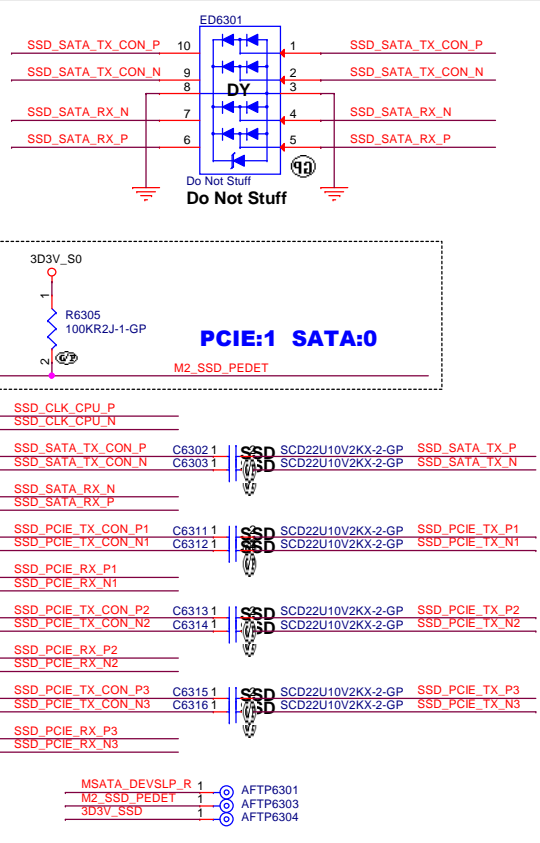
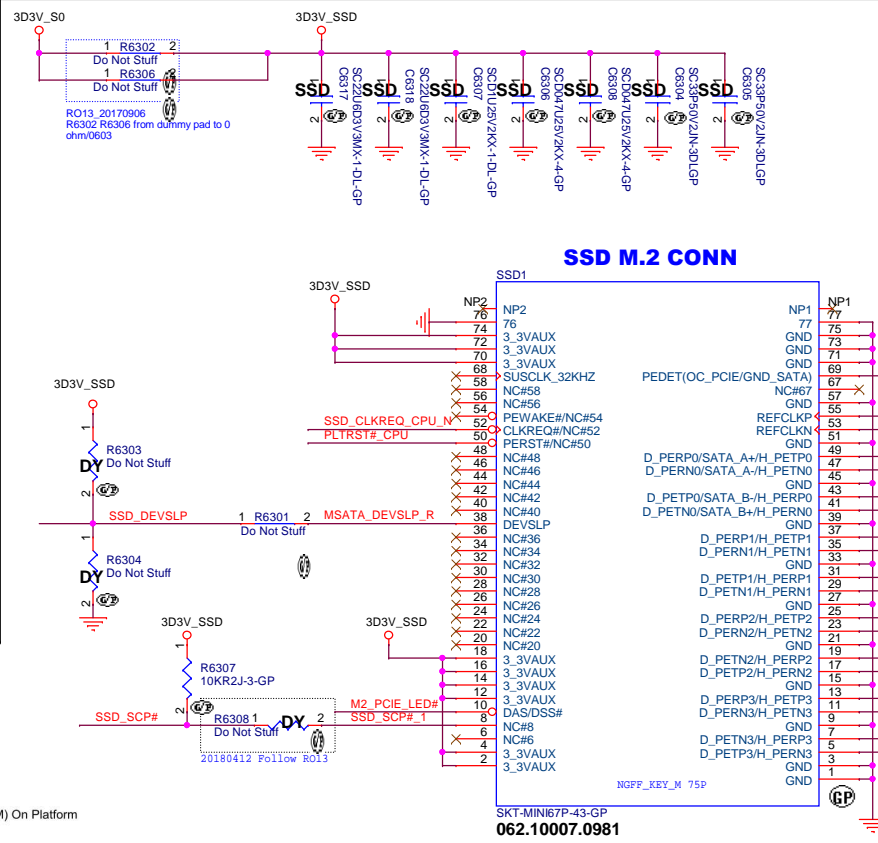
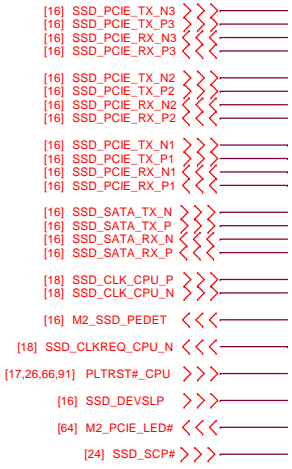


Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

74	SSD_PCIE_TX_N3	SSD_PCIE_TX_N3	75
72	SSD_PCIE_TX_P3	SSD_PCIE_TX_P3	73
68	SSD_PCIE_RX_N3	SSD_PCIE_RX_N3	69
66	SSD_PCIE_RX_P3	SSD_PCIE_RX_P3	67
58	SSD_PCIE_TX_N1	SSD_PCIE_TX_N1	57
54	SSD_PCIE_TX_P1	SSD_PCIE_TX_P1	55
52	SSD_PCIE_RX_N1	SSD_PCIE_RX_N1	53
50	SSD_PCIE_RX_P1	SSD_PCIE_RX_P1	49
46	SSD_SATA_TX_N	SSD_SATA_TX_N	45
44	SSD_SATA_TX_P	SSD_SATA_TX_P	43
42	SSD_SATA_RX_N	SSD_SATA_RX_N	41
40	SSD_SATA_RX_P	SSD_SATA_RX_P	39
38	SSD_CLK_CPU_P	SSD_CLK_CPU_P	37
36	SSD_CLK_CPU_N	SSD_CLK_CPU_N	35
34	SSD_DEVSLP	SSD_DEVSLP	33
32	SSD_PCIE_LED#	SSD_PCIE_LED#	31
30	SSD_SCP#	SSD_SCP#	29
28	SSD_PCIE_TX_N2	SSD_PCIE_TX_N2	27
26	SSD_PCIE_TX_P2	SSD_PCIE_TX_P2	25
24	SSD_PCIE_RX_N2	SSD_PCIE_RX_N2	23
22	SSD_PCIE_RX_P2	SSD_PCIE_RX_P2	21
20	SSD_PCIE_TX_N3	SSD_PCIE_TX_N3	19
18	SSD_PCIE_TX_P3	SSD_PCIE_TX_P3	17
16	SSD_PCIE_RX_N3	SSD_PCIE_RX_N3	15
14	SSD_PCIE_RX_P3	SSD_PCIE_RX_P3	13
12	SSD_PCIE_TX_N1	SSD_PCIE_TX_N1	11
10	SSD_PCIE_TX_P1	SSD_PCIE_TX_P1	9
8	SSD_PCIE_RX_N1	SSD_PCIE_RX_N1	7
6	SSD_PCIE_RX_P1	SSD_PCIE_RX_P1	5
4	SSD_SATA_TX_N	SSD_SATA_TX_N	3
2	SSD_SATA_TX_P	SSD_SATA_TX_P	1

Table 13-11.SATA / PCI Express\* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF <sup>2</sup>	None	None <sup>3</sup>

**Notes:**

- Design Constraint: For PCIe only application, refer to the PCIe guidelines for details.
- Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
- Design Constraint: For PCIe\* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraint: For PCIe\* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraints, Required: Refer to the Chapter 3, "General Differential Signals Design Guidelines" along with the additional guidelines in this section for all design optimization guidelines.
- Design Constraint: For PCIe\* lane that needs to support either **PCIe\* Gen2 devices** or **PCIe\* Gen3 devices**, follow the PCIe\* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

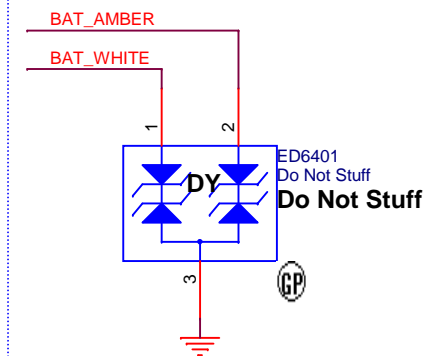
**Important!** SATA Host DEVSLP signals shall not be terminated since device shall terminate the signal.

- This is an open-drain pin on the PCH side. PCH will tri-state this pin to signal to the SATA device that it may enter a lower power state (pin will go high due to pull-up that's internal to the SATA device, per DEVSLP specification). PCH will drive pin low to signal an exit from DEVSLP state.
- When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.

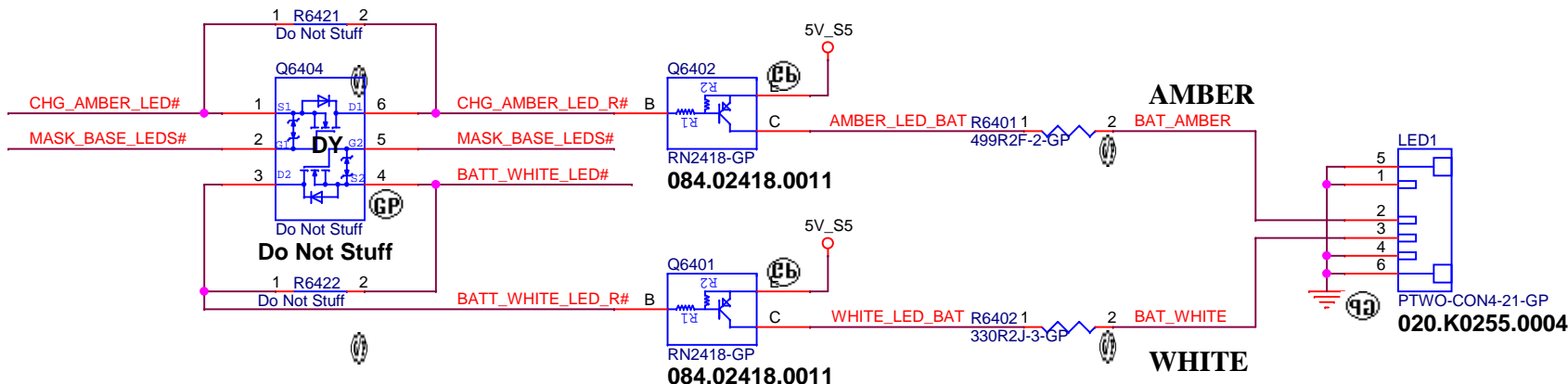
# SSID = Power BTN

[24] CHG\_AMBER\_LED# >>> \_\_\_\_\_  
[24] BATT\_WHITE\_LED# >>> \_\_\_\_\_  
[24] SYS\_LED\_MASK# >>> \_\_\_\_\_  
[16] PCH\_SATA\_LED# >>> \_\_\_\_\_  
[63] M2\_PCIE\_LED# >>> \_\_\_\_\_  
[24,67] LID\_CL\_SIO# >>> \_\_\_\_\_  
[24] MASK\_SATA\_LED#>>> \_\_\_\_\_

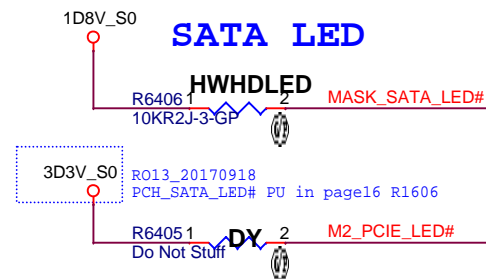
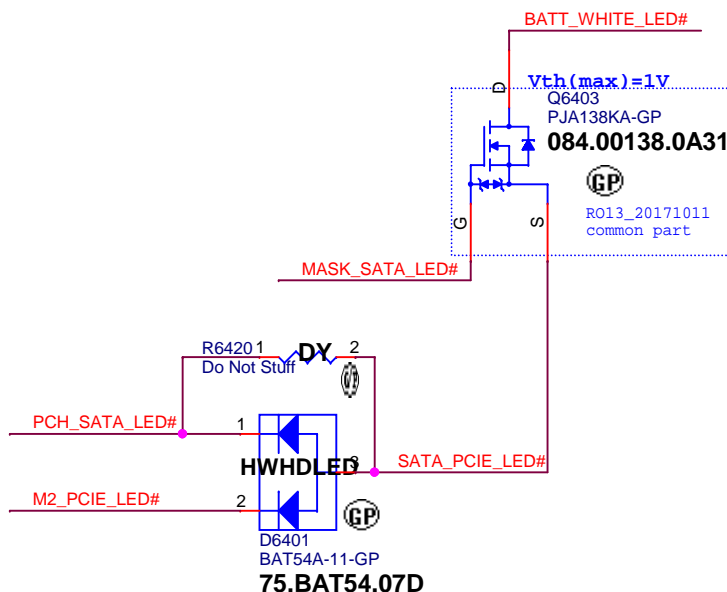
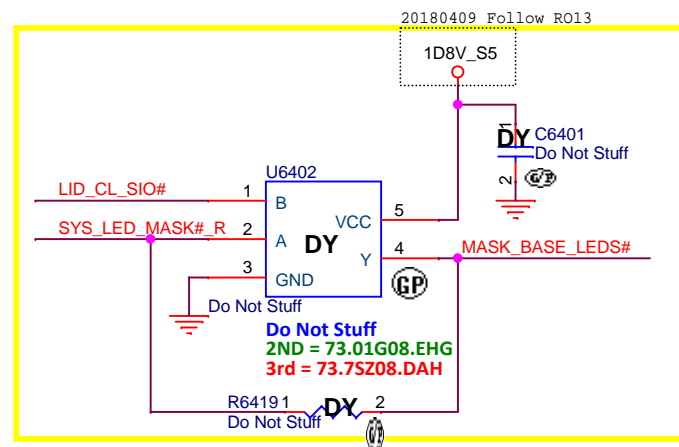
RO13\_20171001 EMI request



## Battery LED1 (AMBER\_LED) Low actived from KBC GPIO



## Battery LED2 (WHITE\_LED) Low actived from KBC GPIO



<Core Design>



Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title

LED Board&Power Button

Size

Document Number

Rev

KR CS MLK 13"

A00

Date: Thursday, July 19, 2018

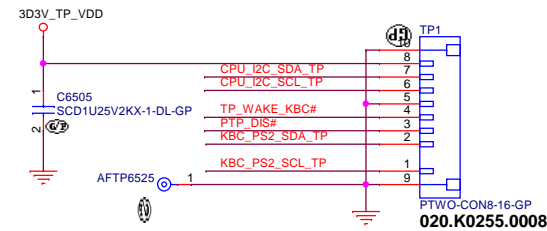
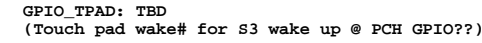
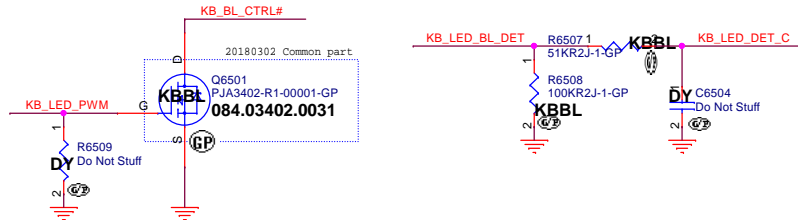
Sheet 64 of 106

```

[24] KSIO[0..7] >>>
[24] KSO[0][0..16] <<<
CPU_I2C_SDA_P0 <<<
CPU_I2C_SCL_P0 <<<
[24] TP_EN# >>>
[20] KB_DET# <<<
[24] PTP_DIS# >>>
[24] KB_LED_PWM >>>
KB_LED_PLB_DET <<<
[24] CAP_LED#_R >>>
CLK_TP_SIO <<<
DAT_TP_SIO <<<
TP_WAKE_KBC# <<<

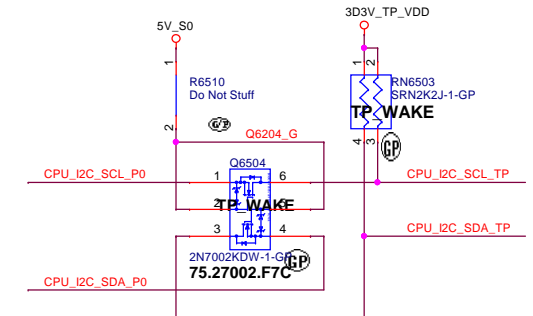
```

Part Number	Pin Number	Signal Name
AFTP6502	1	KS17
AFTP6503	2	KS16
AFTP6505	3	KS14
AFTP6508	4	KS12
AFTP6506	5	KS15
AFTP6501	6	KS11
AFTP6509	7	KS13
AFTP6512	8	KS10
AFTP6510	9	KS05
AFTP6514	10	KS04
AFTP6515	11	KS07
AFTP6517	12	KS06
AFTP6516	13	KS08
AFTP6518	14	KS03
AFTP6511	15	KS01
AFTP6513	16	KS02
AFTP6507	17	KS00
AFTP6519	18	KS12
AFTP6539	19	KS016
AFTP6524	20	KS015
AFTP6520	21	KS013
AFTP6521	22	KS014
AFTP6504	23	KS09
AFTP6522	24	KS011
AFTP6523	25	KS010
AFTP6538	26	CAP_LED
	27	
	28	
	29	
	30	
	31	

[illegible]

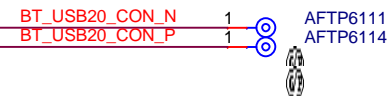
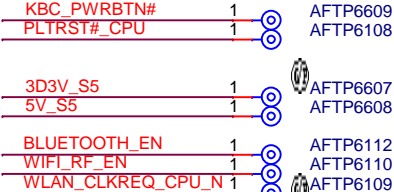
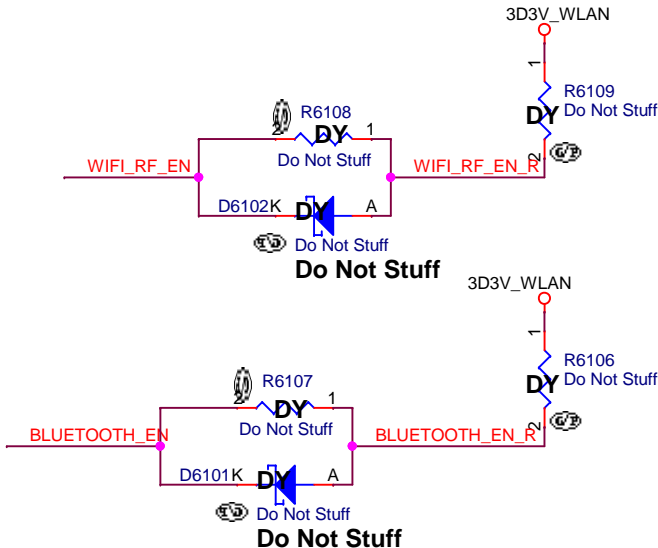
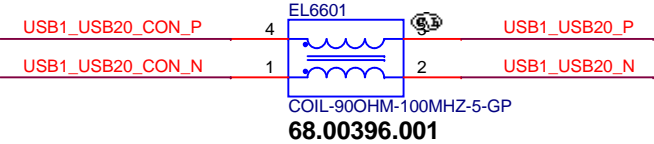
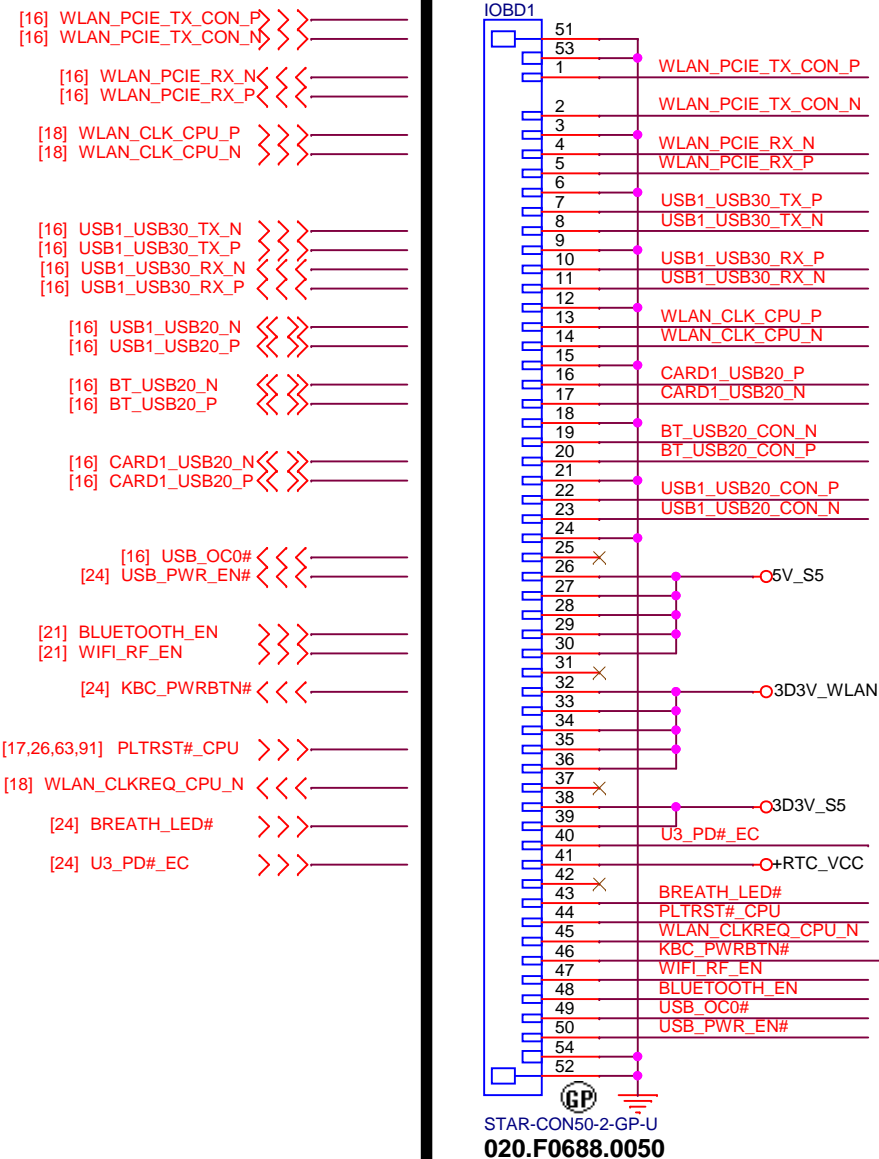
Pin number	Pin name
1	VDD
2	DAT (I2C)
3	CLK (I2C)
4	GND
5	ATTN
6	GPIO
7	DAT (PS2)
8	CLK (PS2)

3D3V_TP_VDD	1	AFTP6537
KBC PS2_SCL_TP	1	AFTP6538
KBC PS2_SDA_TP	1	AFTP6539
CPU_I2C_SCL_TP	1	AFTP6540
CPU_I2C_SDA_TP	1	AFTP6541
TP_WAKE_KBC#	1	AFTP6542
PTP_DIS#	1	AFTP6543



Title			
<b>Key Board&amp;Touch Pad</b>			
Size A3	Document Number	Rev	
	<b>KR CS MLK 13"</b>	<b>A00</b>	
Date:	Thursday, July 19, 2018	Sheet 65 of	106

SSID = IO Connector



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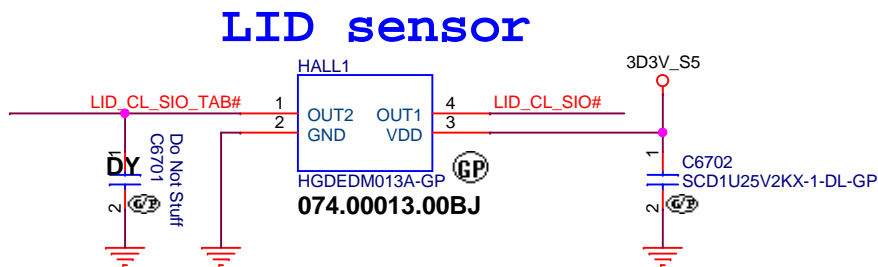
Title  
**IO Board Connector**

Size A4 Document Number  
**KR CS MLK 13"**

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# SSID = Hall Sensor

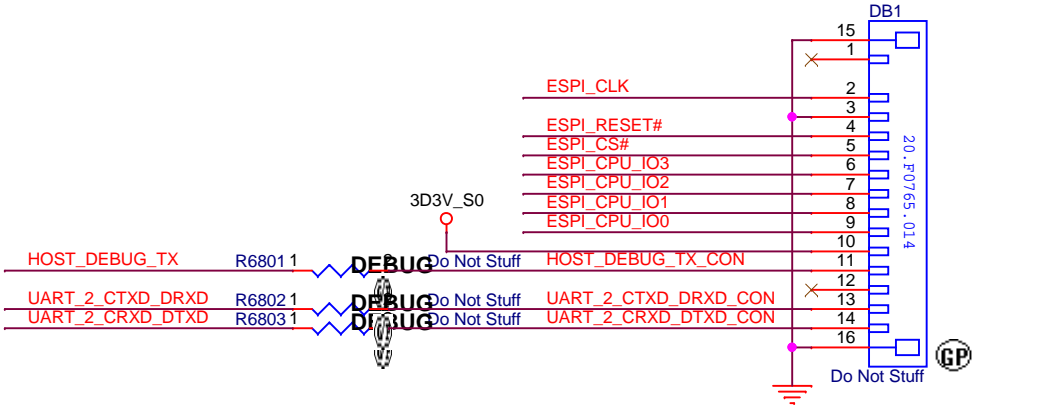
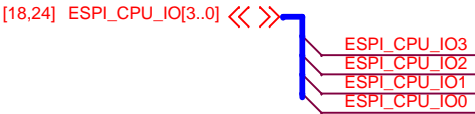
[24,64] LID\_CL\_SIO# <<<—  
[24] LID\_CL\_SIO\_TAB# <<<—



<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Hall Sensor</b>			
Size A4	Document Number <b>KR CS MLK 13"</b>		Rev <b>A00</b>
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SSID = Debug



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Title

**Dubug connector**

Size  
A4

Document Number  
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Rev  
**A00**

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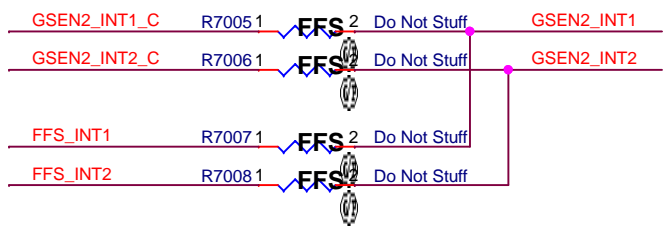
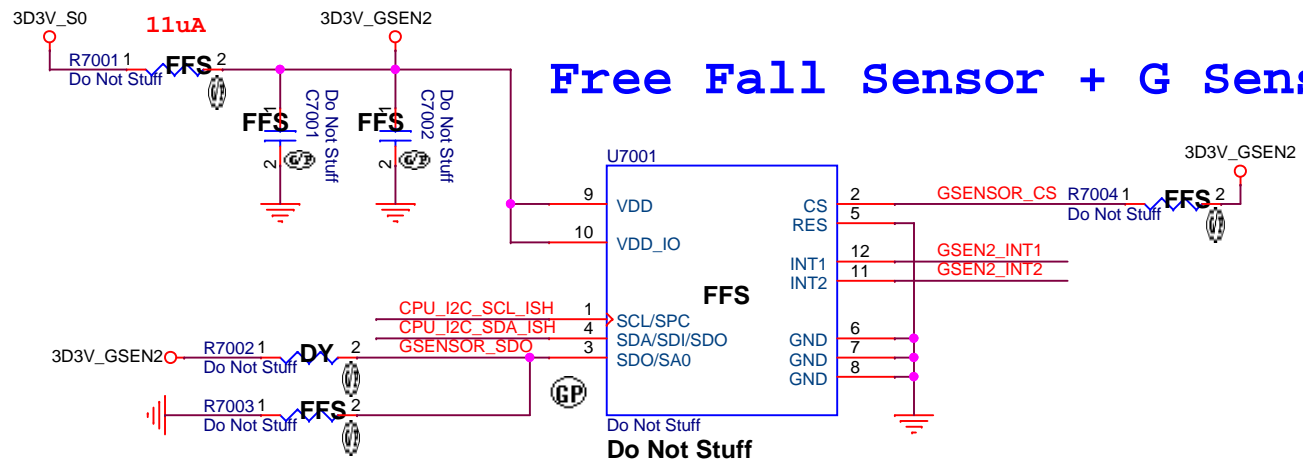
( Blanking )

<Core Design>


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Title			
<b>Reserved</b>			
Size A4	Document Number <b>KR CS MLK 13"</b>		Rev <b>A00</b>
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SSID = Free Fall Sensor

[20] GSEN2\_INT1\_C <<<<  
[20] GSEN2\_INT2\_C <<<<  
[18] FFS\_INT1 <<<<  
[20] FFS\_INT2 <<<<  
[20,55] GYRO\_INT\_C <<<  
[20,55] CPU\_I2C\_SDA\_ISH <<<<  
[20,55] CPU\_I2C\_SCL\_ISH <<<<



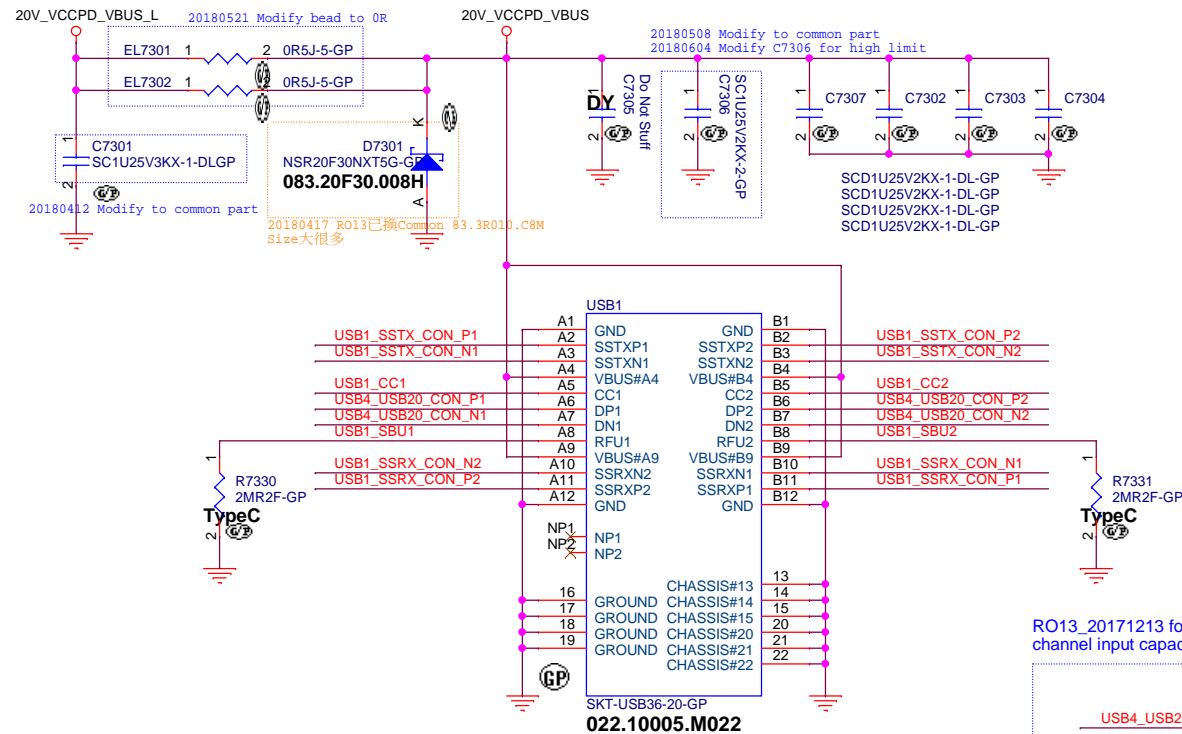
<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Sensor (G-sensor)</b>			
Size A4	Document Number <b>KR CS MLK 13"</b>		Rev <b>A00</b>
Date: Thursday, July 19, 2018		Sheet 70 of 106	

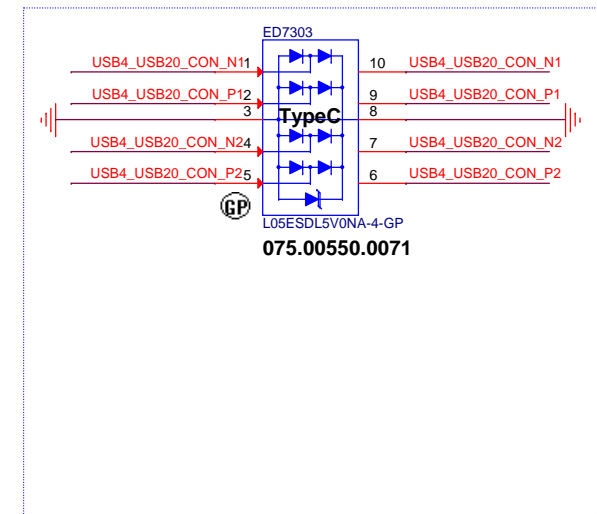




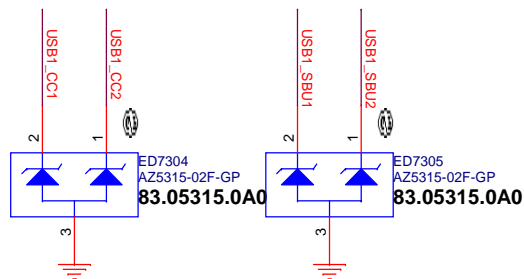
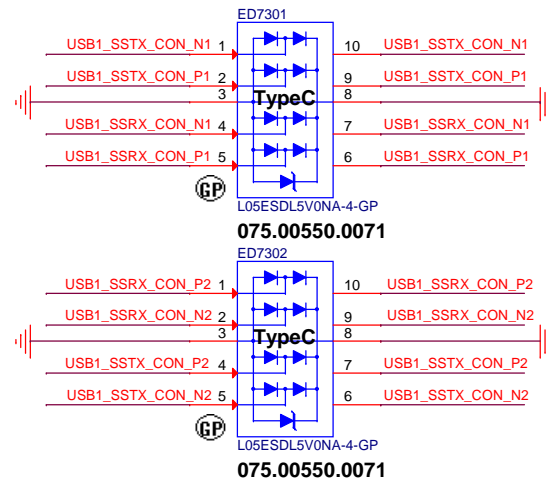
**SSID = TYPEC CONNECTOR**



RO13\_20171213 for EMI request  
channel input capacitance max.0.3pF(075.00550.0071)



20180110 Follow RO13 to remove RX RC



## <Core Design>



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Title
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**GPU(1/5)PEG**

Size	
Custom	

Document Number

**KR CS MLK 13"**

Rev  
A00

Date: Thursday, July 19, 2018

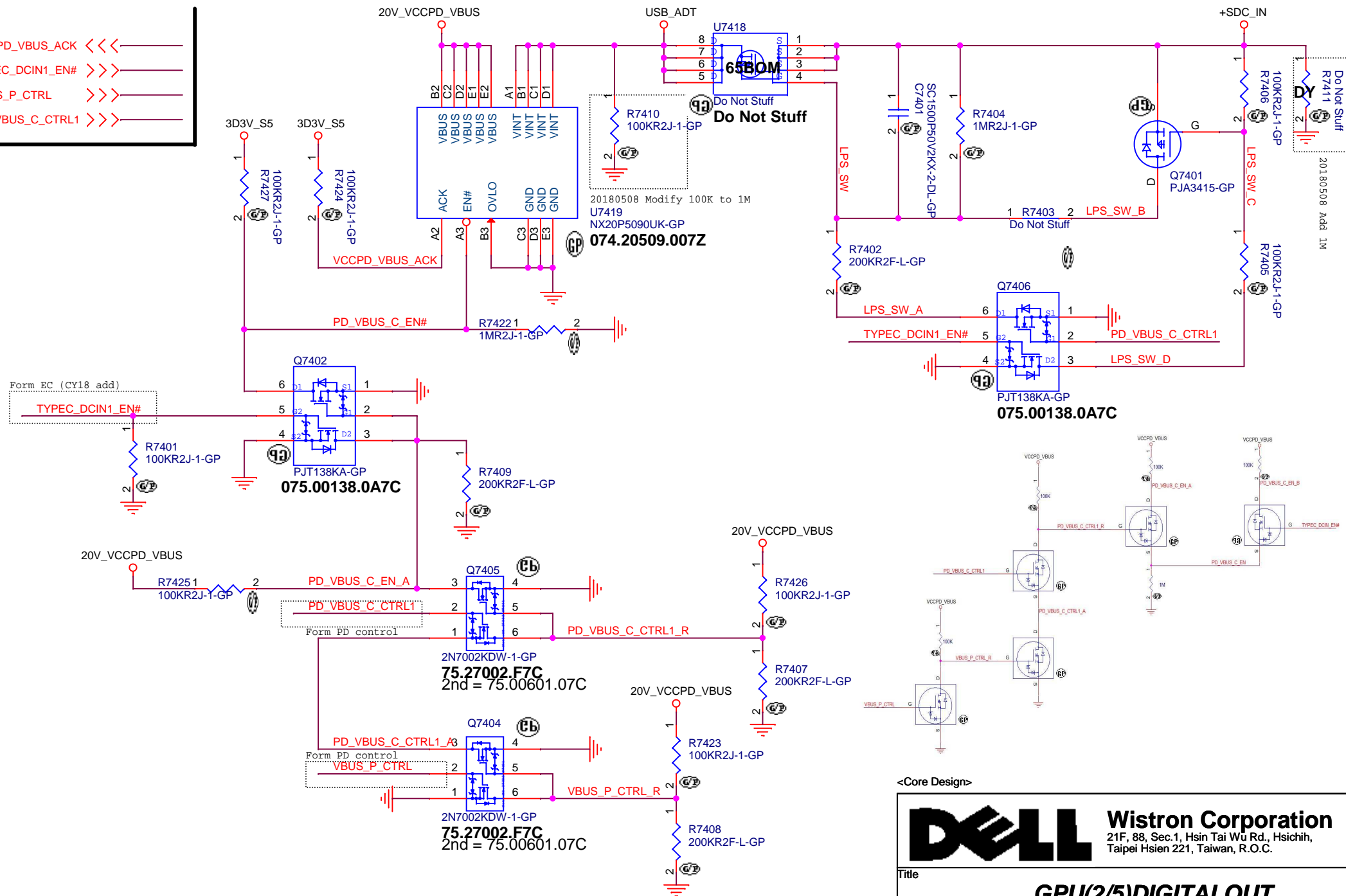
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106

## Main Func = Type-C LPS

```
[44] VCCPD_VBUS_ACK <<<_____
[24] TYPEC_DCIN1_EN# >>>_____
[72] VBUS_P_CTRL >>>_____
[72] PD_VBUS_C_CTRL1 >>>_____
```



## <Core Design>



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Title	Author	Year	Journal	Volume	Issue	Page
1. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	1-15
2. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	16-30
3. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	31-45
4. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	46-60
5. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	61-75
6. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	76-90
7. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	91-105
8. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	106-120
9. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	121-135
10. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	136-150

**GPU(2/5)DIGITALOUT**

Size  
A4

Document Number

**KR CS MLK 13"**

Rev

**A00**

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106

Main Func = dGPU

( Blanking )

<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>GPU(3/5)VRAM/F</b>		
Size A4	Document Number <b>KR CS MLK 13"</b>	Rev <b>A00</b>
Date: Thursday, July 19, 2018		Sheet 75 of 106

Main Func = dGPU

( Blanking )

<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>GPU(4/5)GPIO/STRAP</b>			
Size A4	Document Number <b>KR CS MLK 13"</b>		Rev <b>A00</b>
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Main Func = dGPU

(Blanking)

<Core Design>



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Title

**GPU(5/5)PWR/GND**

Size  
A4

Document Number

**KR CS MLK 13"**

Rev  
**A00**


Date: Thursday, July 19, 2018

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SSID = VRAM

( Blanking )


<Core Design>

			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
GPU-VRAM1,2 (1/4)					
Size	Document Number				Rev
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Date: Thursday, July 19, 2018		Sheet 78		of 106	

SSID = VRAM

(Blanking)

<Core Design>



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Title

**GPU-VRAM3,4 (2/4)**

Size

A4

Document Number

**KR CS MLK 13"**

Rev

**A00**

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Main Func = dGPU

(Blanking)

<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>GPU(5/5)PWR/GND</b>			
Size A4	Document Number <b>KR CS MLK 13"</b>		Rev <b>A00</b>
Date: Thursday, July 19, 2018		Sheet 80 of	106

Main Func = dGPU

( Blanking )

<Core Design>



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Title

**GPU-VRAM1,2 (1/4)**

Size  
A4

Document Number  
**KR CS MLK 13"**

Rev  
**A00**

Date: Thursday, July 19, 2018

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Main Func = dGFX\_CORE

( Blanking )

<Core Design>



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Title

**RT8812 VGACORE**

Size  
A4

Document Number

**KR CS MLK 13"**

Rev  
**A00**

Date: Thursday, July 19, 2018

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Main Func = dGPU

( Blanking )

<Core Design>

			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>DISCRETE VGA POWER</b>					
Size A4	Document Number <b>KR CS MLK 13"</b>				Rev <b>A00</b>
Date: Thursday, July 19, 2018		Sheet 83 of		106	

Main Func = dGPU

( Blanking )

<Core Design>



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Title

**GPU-VRAM7,8 (4/4)**

Size  
A4

Document Number  
**KR CS MLK 13"**

Rev  
**A00**

Date: Thursday, July 19, 2018

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Main Func = dGFX\_CORE

(Blanking)

<Core Design>



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Title

**GPU CORE**

Size  
A4

Document Number  
**KR CS MLK 13"**

Rev  
**A00**


Date: Thursday, July 19, 2018

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Main Func = dGPU

( Blanking )

<Core Design>



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Title

**GPU Discrete Power**

Size  
A4

Document Number  
**KR CS MLK 13"**

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**A00**

Date: Thursday, July 19, 2018

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( Blanking )

<Core Design>



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Title

***Reserved***

Size  
A4

Document Number

***KR CS MLK 13"***

Rev

***A00***

Date: Thursday, July 19, 2018

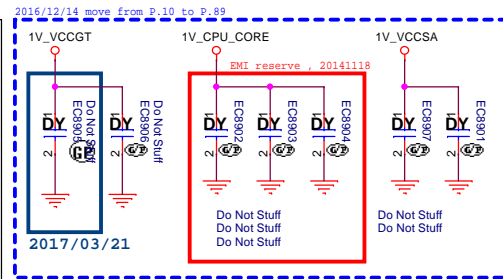
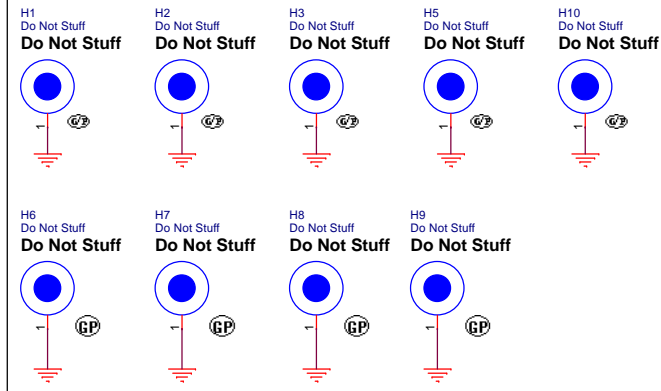
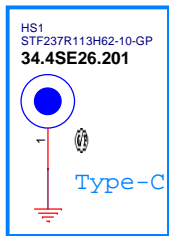
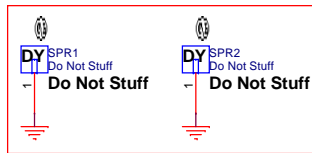
Sheet 87 of 106

( Blanking )

<Core Design>

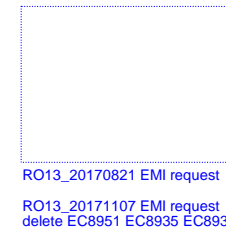
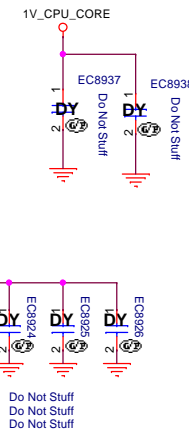
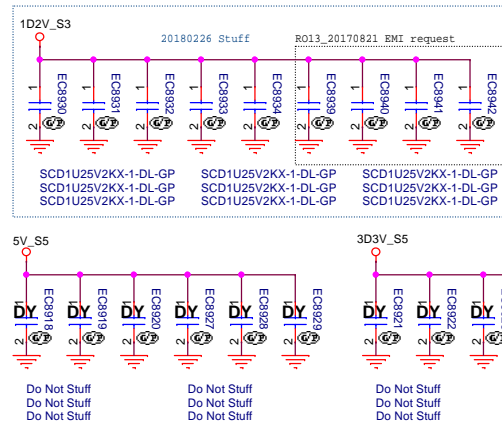
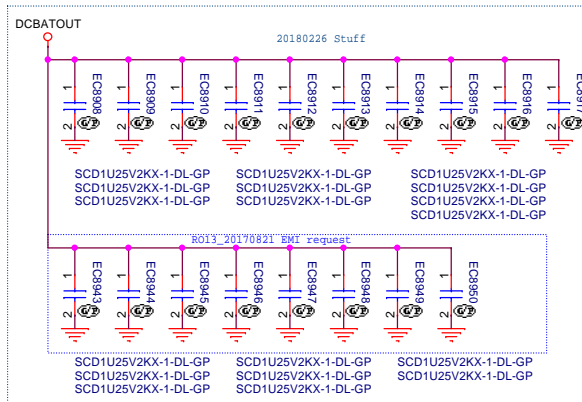
			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
<b>Reserved</b>					
Size	Document Number				Rev
A4	<b>KR CS MLK 13"</b>				<b>A00</b>
Date: Thursday, July 19, 2018			Sheet	88	of 106

## SSID = Unused Parts

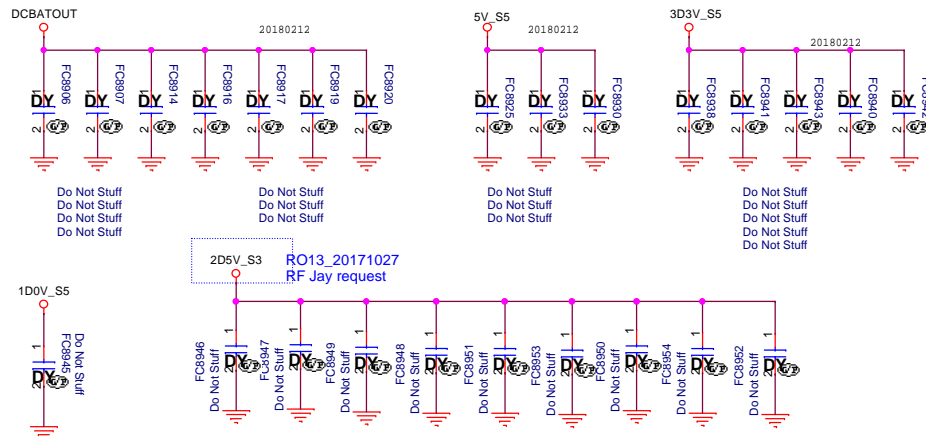


## SSID = EMI

Mind the voltage rating of the caps.



## SSID = RF



( Blanking )

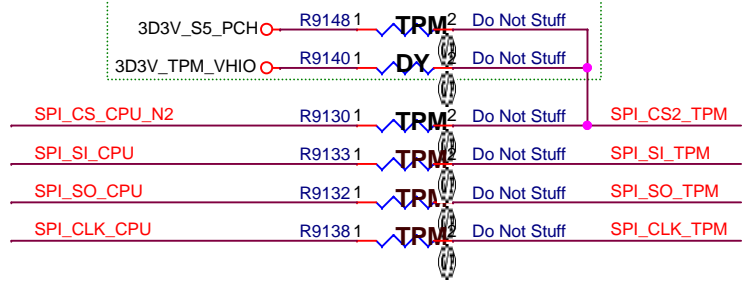
<Core Design>

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Title			
<b>Reserved</b>			
Size A4	Document Number <b>KR CS MLK 13"</b>		Rev <b>A00</b>
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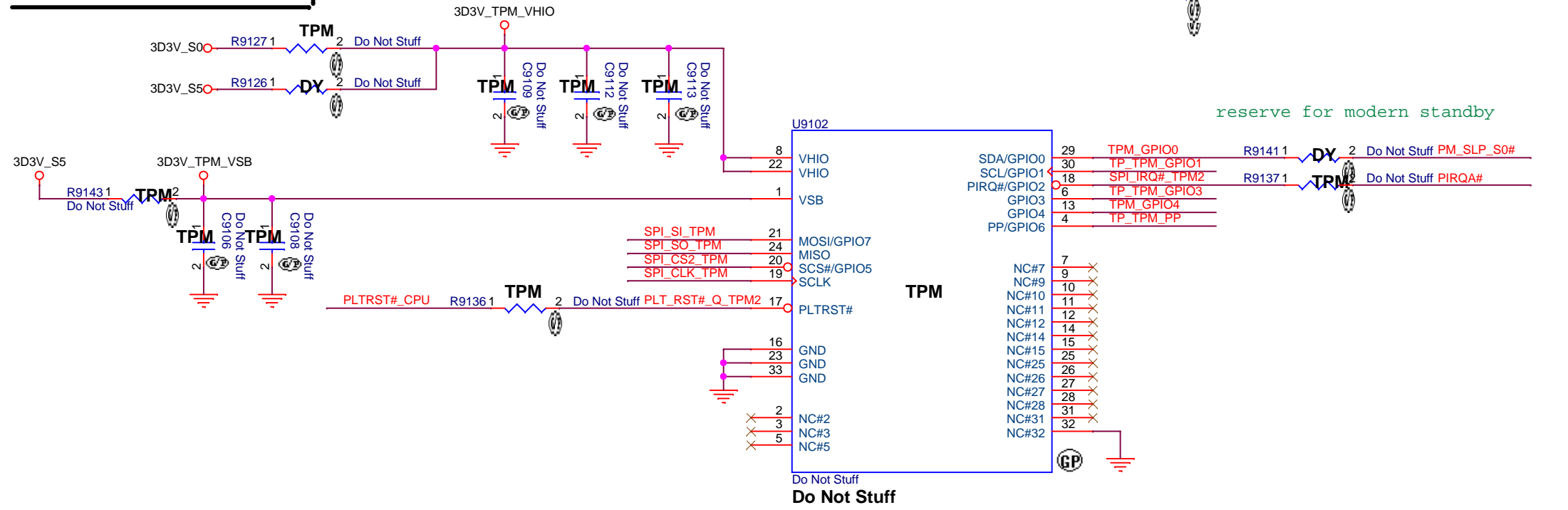
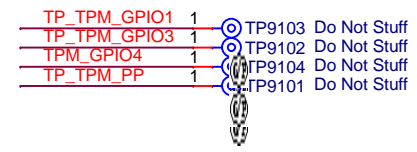
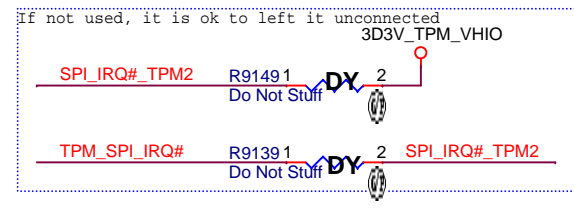
SSID = TPM

- [20] PIRQA# >>>
- [18] TPM\_SPI\_IRQ# >>>
- [17,26,63,66] PLTRST#\_CPU >>>
- [17,40] PM\_SLP\_S0# >>>
- [18] SPI\_CS\_CPU\_N2 >>>
- [18,25] SPI\_SO\_CPU <<<
- [15,18,25] SPI\_SI\_CPU >>>
- [18,25] SPI\_CLK\_CPU >>>

reserve RTC Gen 9 reset circuit\_20170814  
leakage issue




EVT Reseved RO13\_20171005



reserve for modern standby

<Core Design>



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Title

TPM2.0

Size  
A4

Document Number  
KR CS MLK 13"

Rev  
A00

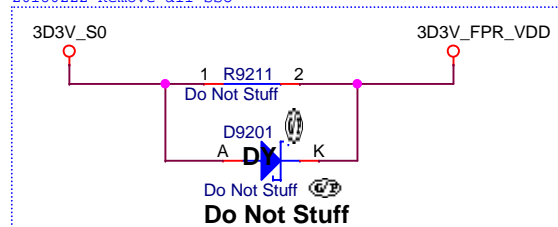
Date: Thursday, July 19, 2018

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SSID = FPR

[16] FP1\_USB20\_P >>>  
[16] FP1\_USB20\_N >>>  
[24] FPR\_SCAN# >>>

20180222 Remove all SSO



## FBR(Botton side finger Print Sensor)

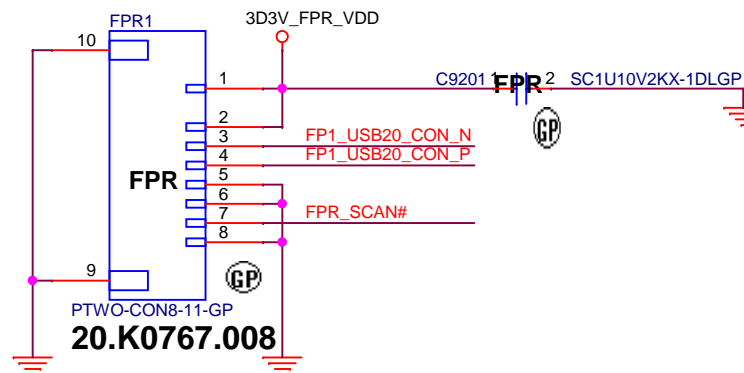
RO13\_20170929  
remove R9212(DY)



## Co-lay CMC and RES

20180211

20180201 Add co-lay CMC



## GF5288WN1+GF128A+GM168 Module design

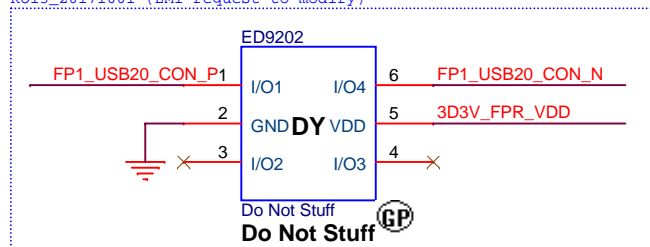
### Pin Definition

#### CN PIN MAP

PIN NO.	INFO
1	VCC-3.3V
2	Power button
3	USB_N
4	USB_P
5	GND
6	LID closed
7	GPIO_key shielding
8	GND(ID pin)

	PM_SLP_S4#	FP_3D3V
S0	1	1
S3	1	1
S4	0	0
S5	0	0

RO13\_20171001 (EMI request to modify)



<Core Design>



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Title <b>(Reserved)Finger Print</b>		
Size A4	Document Number <b>KR CS MLK 13"</b>	Rev <b>A00</b>
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( Blanking )

<Core Design>



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Title

*(Reserved)*

Size  
A4

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( Blanking )

<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>(Reserved)</b>			
Size A4	Document Number <b>KR CS MLK 13"</b>		Rev <b>A00</b>
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<Core Design>

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Title <b>(Reserved)</b>			
Size A4	Document Number <b>KR CS MLK 13"</b>		Rev <b>A00</b>
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<Core Design>

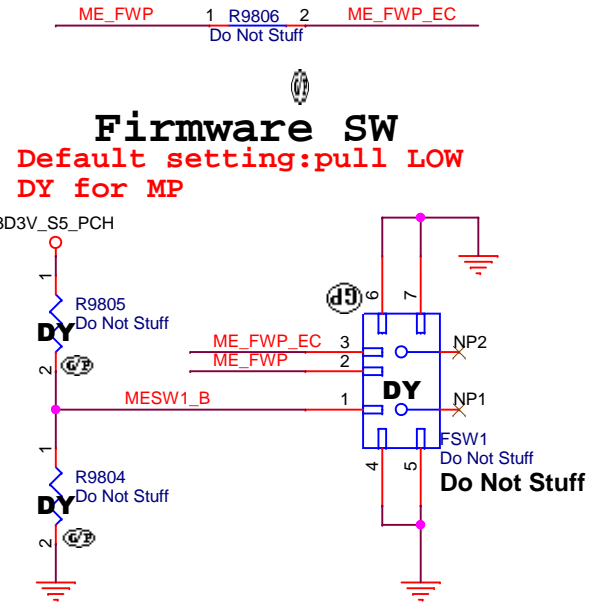
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>(Reserved)</b>			
Size A4	Document Number <b>KR CS MLK 13"</b>		Rev <b>A00</b>
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( Blanking )

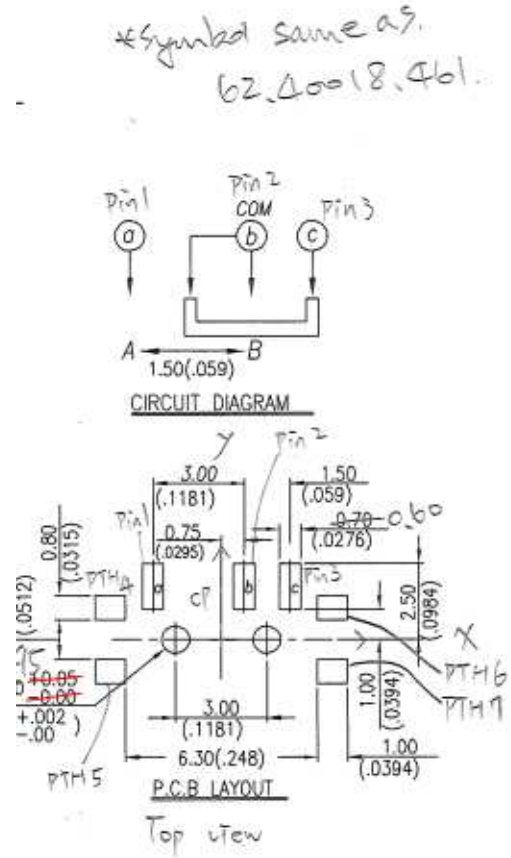
<Core Design>

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Title <b>LVDS Switch</b>			
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[24] ME\_FWP\_EC >>>  
[19] ME\_FWP <<<



	3	1
ME_FWP	LOW Normal Operation (Default)	HIGH Override



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**CRT Switch**

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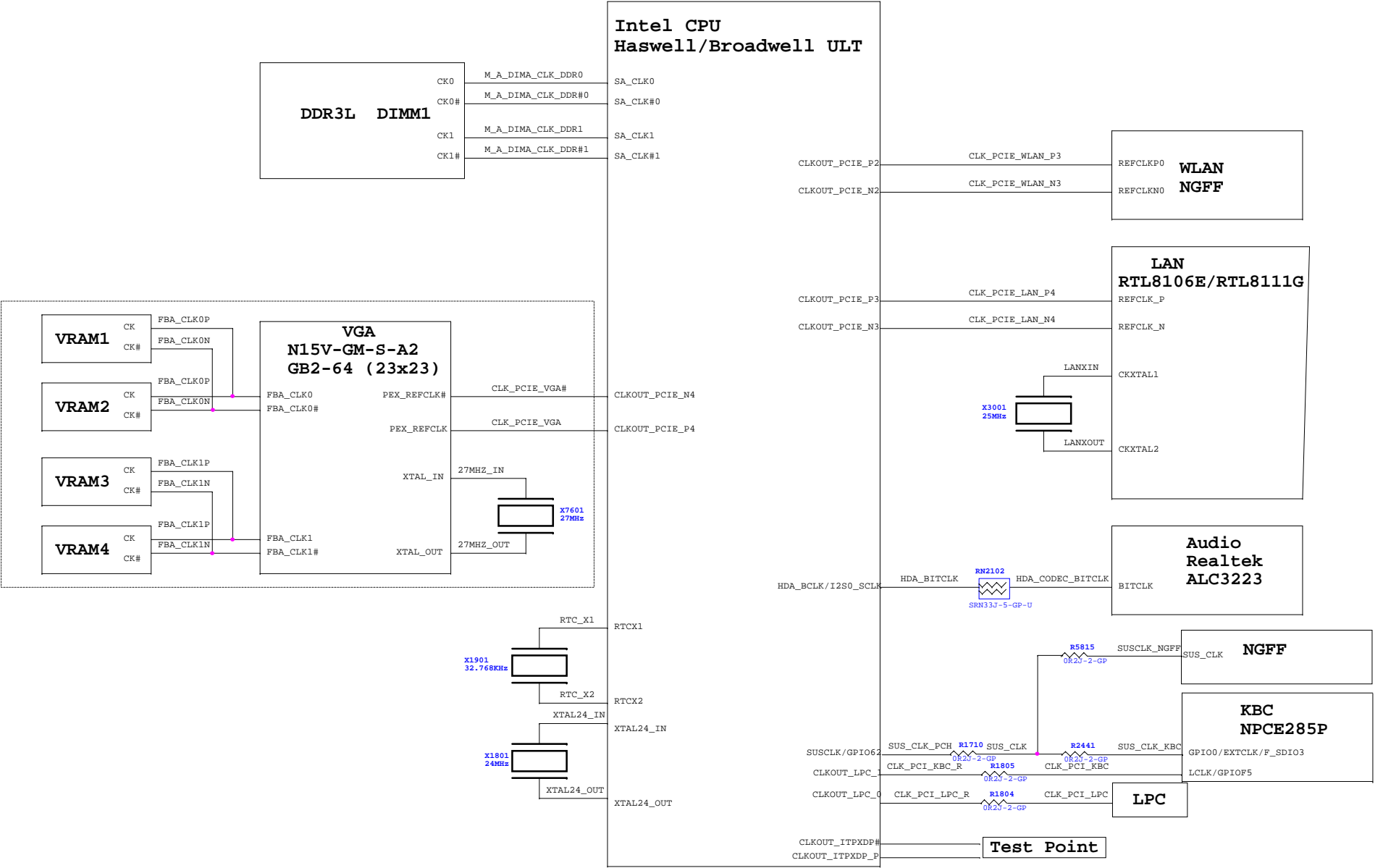
SSID = Debug

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Title <b>CPU XDP;PCH XDP</b>			
Size A4	Document Number <b>KR CS MLK 13"</b>		Rev <b>A00</b>
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CLK Block Diagram

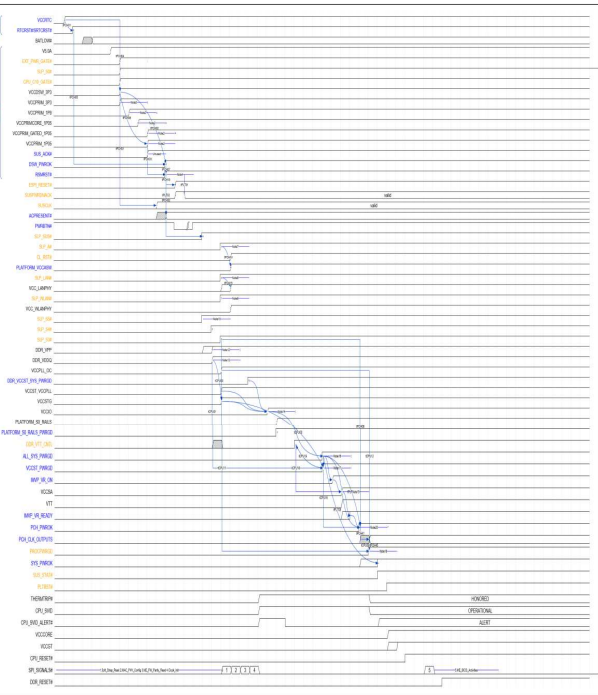




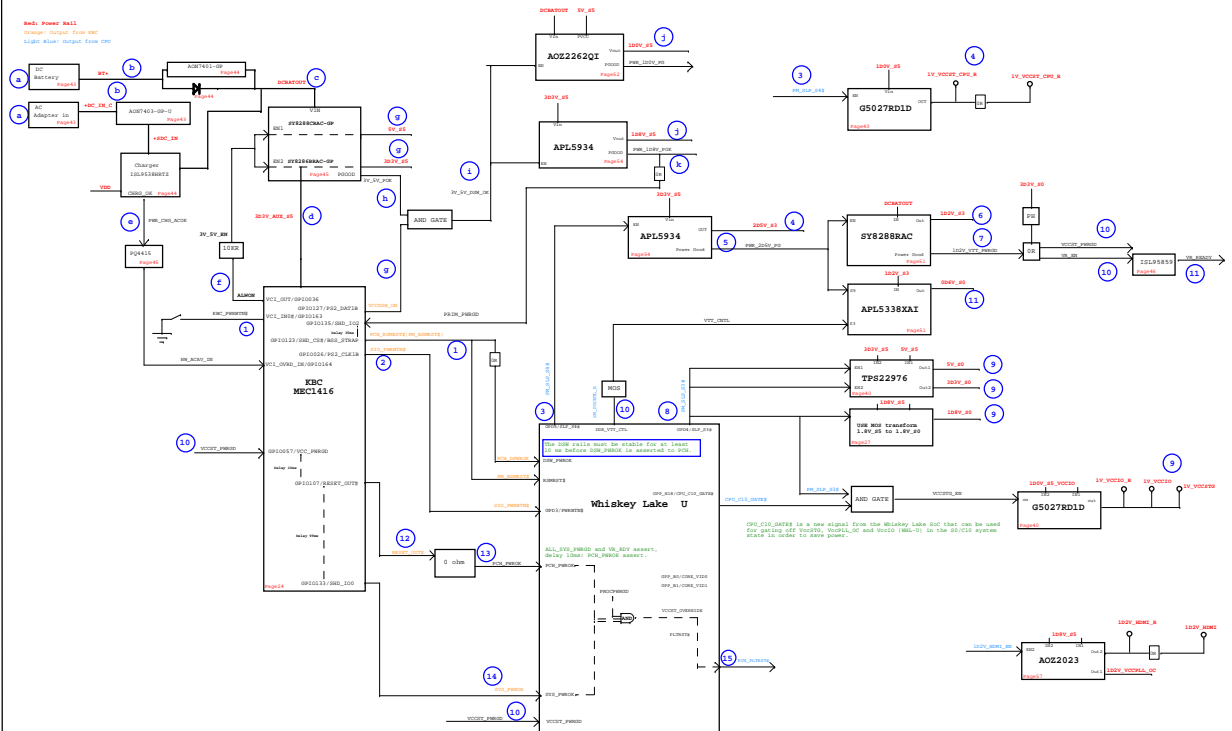
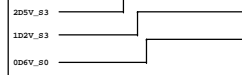
[illegible][illegible]

 <div style="float: right;"> <b>Wistron Corporation</b>                  21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,                  Taipei Hsein 221, Taiwan, R.O.C.             </div>			
Title			
<b><i>Change History</i></b>			
Size A3	Document Number <b><i>KR CS MLK 13"</i></b>	Rev <b><i>A00</i></b>	
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## WHL-U Timing Diagram for G3 to S0/M0 (Non-Deep Sx Platform)



## For DDR4 power sequence



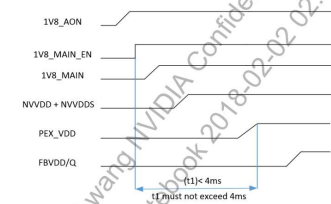
## [dGPU] N16x Power-Up/Down Sequence

### Power-Up Sequence

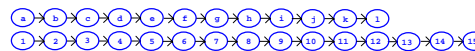
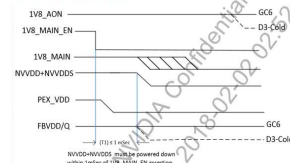
The following power-up sequence is required:

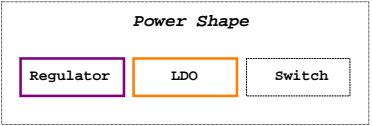
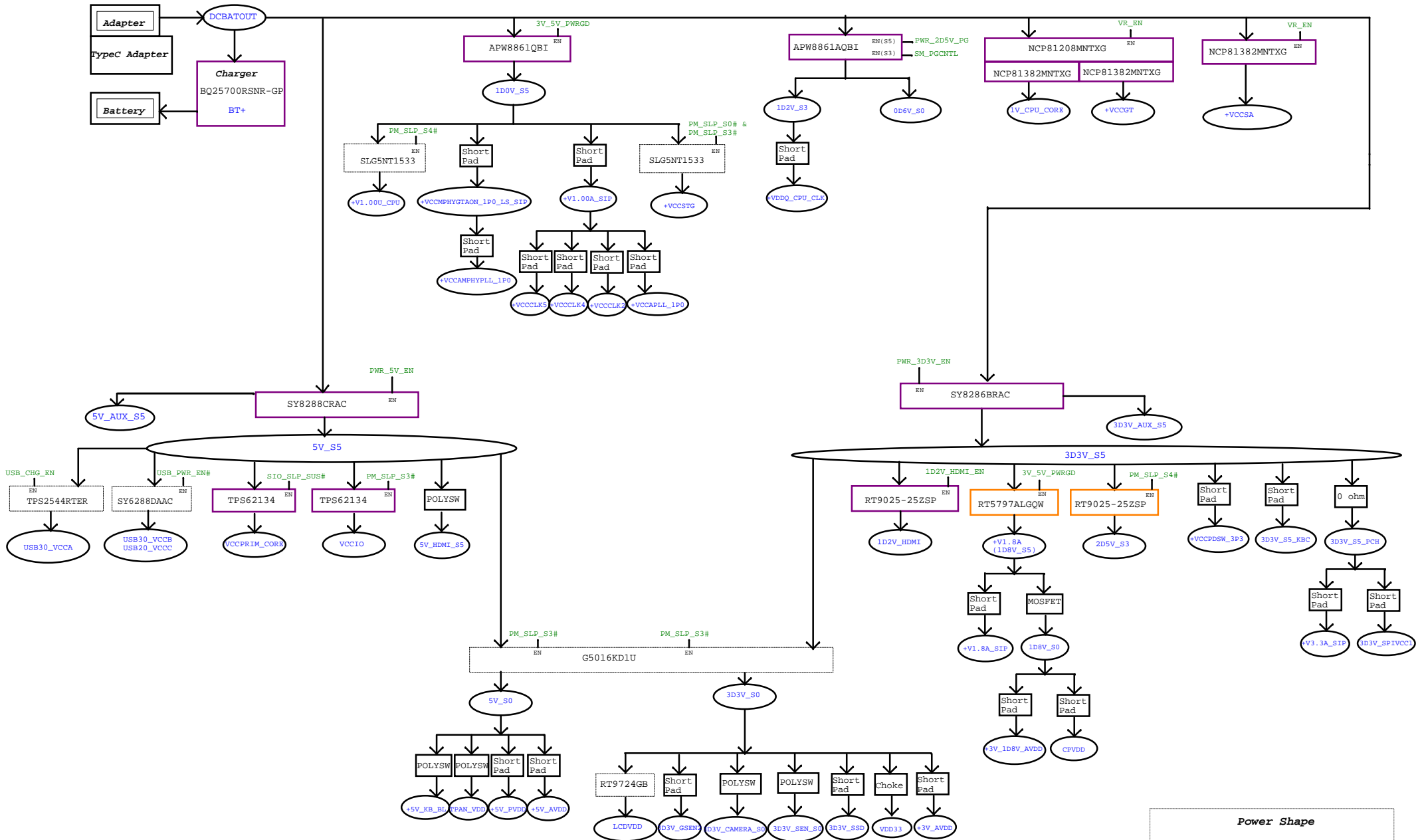
- 1V8\_AON → 1V8\_MAIN → (NVVDD+NVVDD5) → PEX\_VDD → FBVDD/Q
- All CPU power rails must ramp up after 1V8\_AON
- FBVDD/Q should ramp up after (NVVDD+NVVDD5) and PEX\_VDD.

All other 1.8V power rails can ramp up with 1V8\_MAIN including PEX\_VDD and all PLLVDD rails; all other 1V power rails can ramp up with PEX\_VDD.

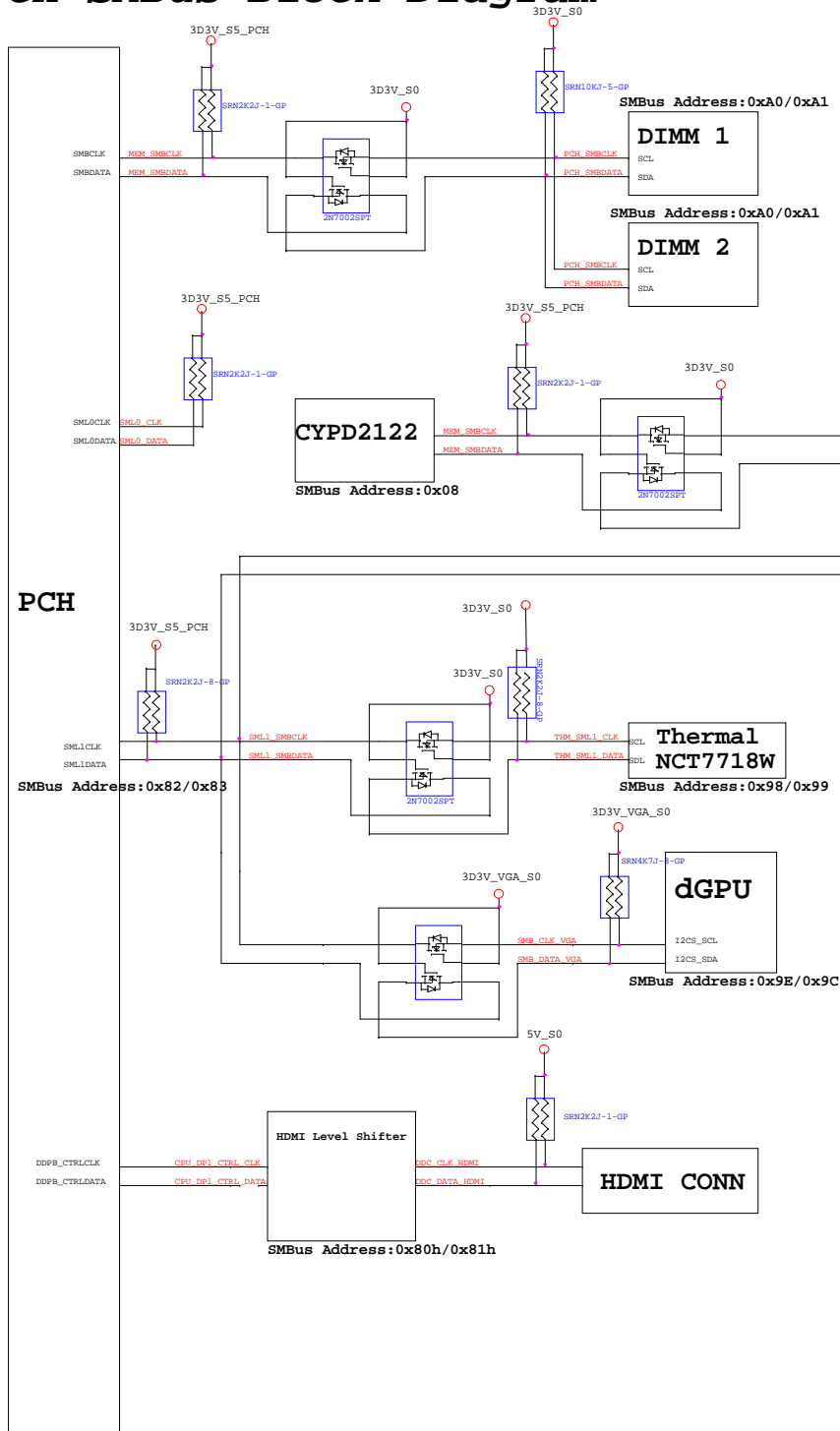


### Power-Down Sequence

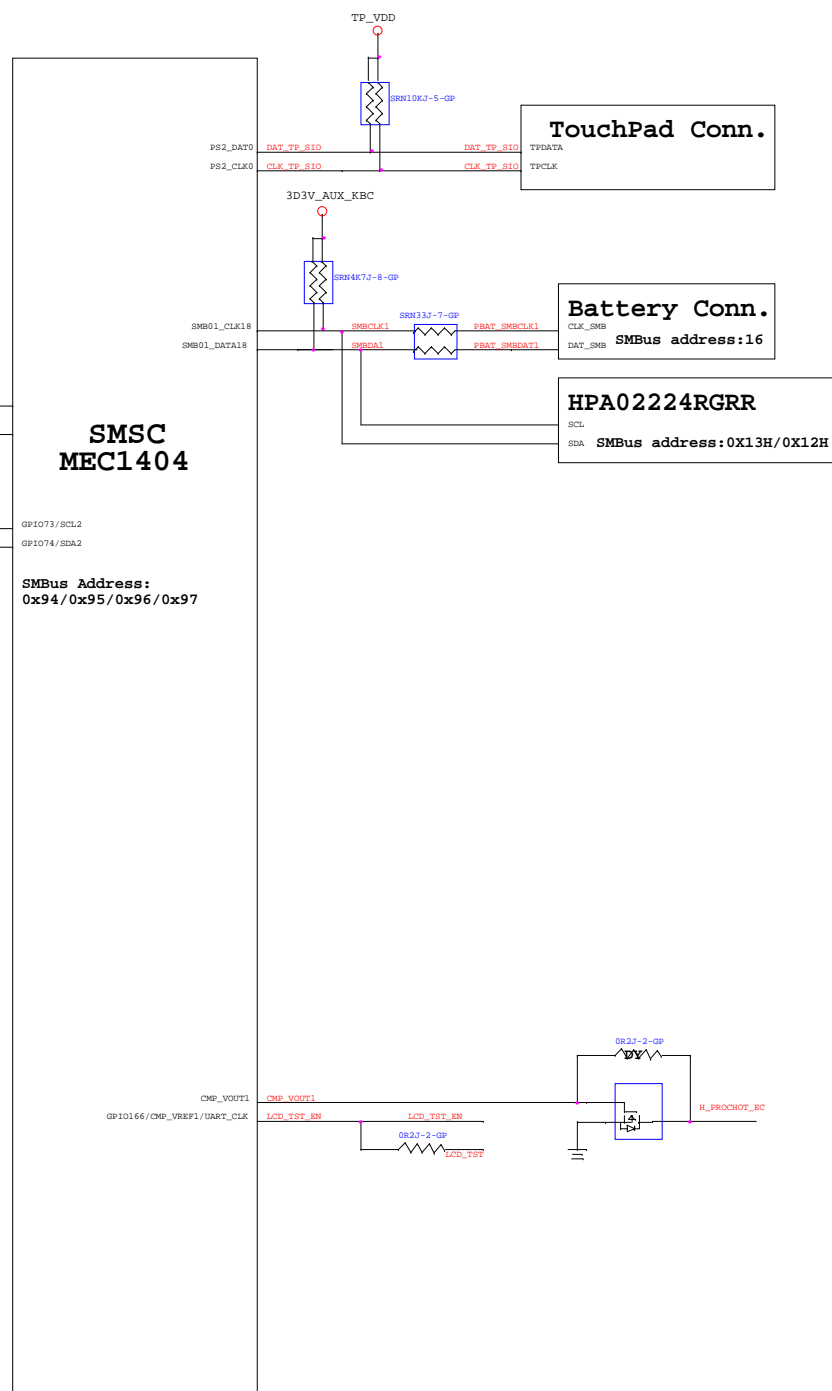




# PCH SMBus Block Diagram

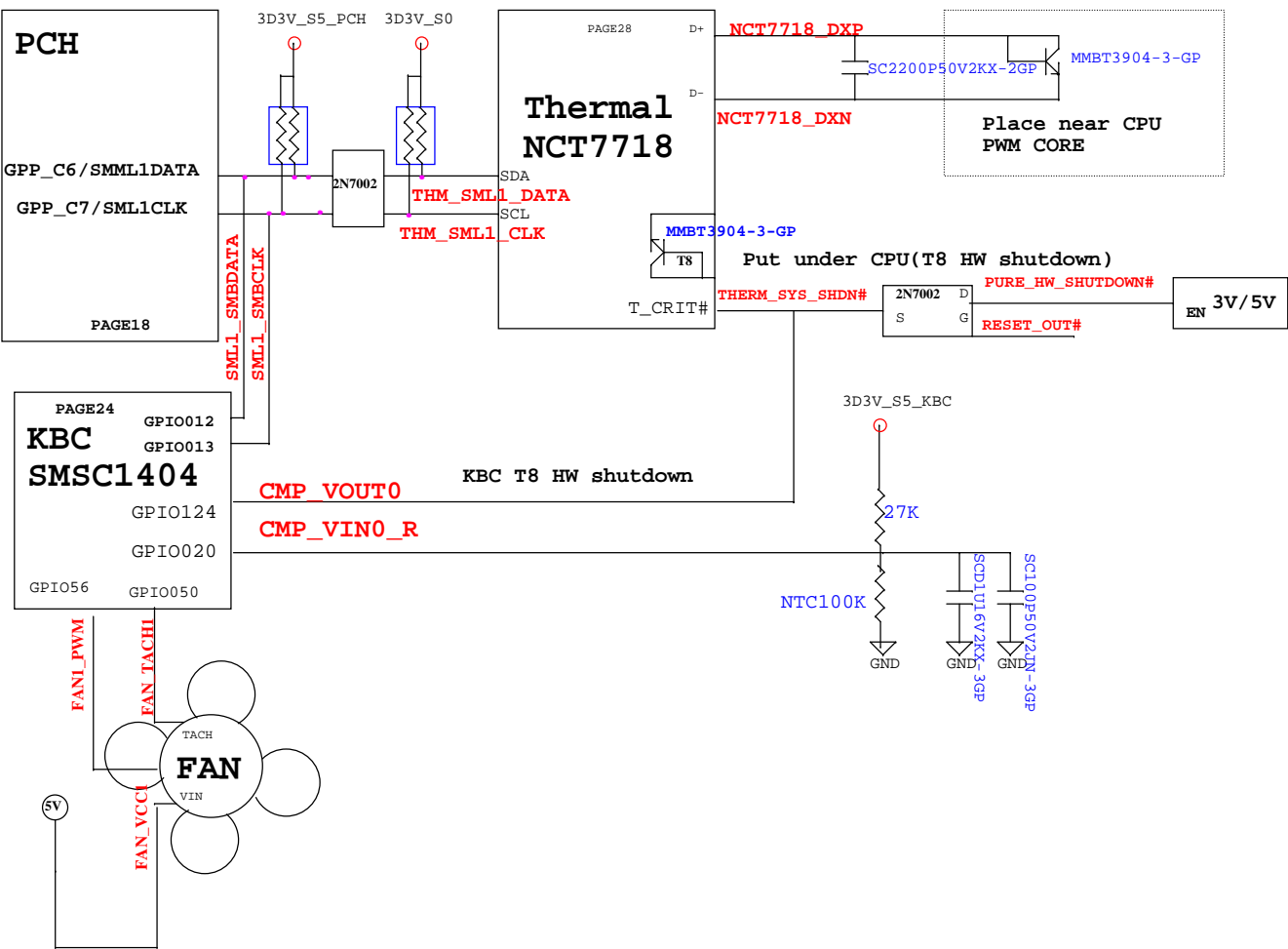


# KBC SMBus Block Diagram

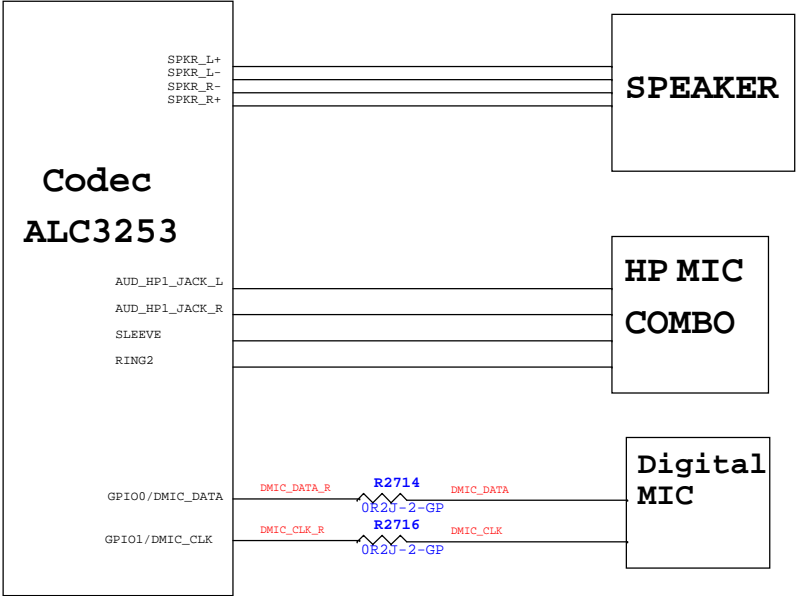


<Core Design>

# Thermal Block Diagram



# Audio Block Diagram



D

C

B

A

## <Core Design>



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## SIP connector

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